A Hybrid Multilevel Inverter Topology with Third Harmonic Injection for Grid Connected Photovoltaic Central Inverters

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Abstract: A three phase hybrid multilevel inverter topology is proposed for grid integrated photovoltaic central inverter systems. This topology is a hybrid of cascaded H bridge topology (CHB) and neutral point clamped (NPC) topology. The inverter uses asymmetric structure of dc bus voltage to increase the number of levels of the inverter. Third harmonic injection is proposed in order to have better utilization of the dc bus and to obtain higher number of levels. Nearest voltage level control is adapted as modulation technique to have good dynamic performance with less computational burden. A 29-level MATLAB/Simulink model of the inverter is developed to verify the performance of the proposed topology. The simulation uses only two H-bridges per phase and one three phase NPC (three-level) inverter to obtain 29 levels in line-to-line voltage. The objective of the work is: Reduction of number of switching devices, system (converter and controller) cost, EMI problem, device losses, and increasing the dynamic performance and efficiency. The proposed topology and its control are simulated using MATLAB/SIMULINK and confirmed through prototype experimentation in the laboratory.

Index Terms: Hybrid multilevel inverter topology, grid connected photovoltaic system, third harmonic injection, nearest voltage level control, asymmetric multilevel inverter.

I. INTRODUCTION

Importance of renewable energies such as solar PV, wind etc. is on the rise due to environmental issues. However, harvesting of renewable energy is a challenge from different perspectives. Firstly, the cost of energy is still high compared to carbon based technology. Added to this is the non-smooth nature of the availability of the energy leading to further need of energy management together with maximum energy capture.

One of the fastest growing renewable energy generation systems is solar PV. The demand of photovoltaic energy is rapidly increasing. As a consequence there is a lot of research going on to increase the efficiency of photovoltaic power plants and to decrease system cost. This work is intended to increase the converter efficiency and reduction of system cost. In present scenario, hundreds of large (Multi Megawatt) photovoltaic power plant is operating across the globe. In 2016, Europe has experienced the maximum installation of photovoltaic (PV) systems (of the level of 13GW) exceeding all other renewable electricity sectors. It is expected that global solar PV installations will reach 24GW in 2017. Attractive support schemes have encouraged the solar PV economy and the cost of solar modules is decreasing. [1].

Grid connected large photovoltaic power plants require to have medium voltage and high current inverter. A simple PWM inverter is having multiple disadvantages to use for grid integration of large photovoltaic system; this will have high device losses, high EMI problem, increasing device stresses and high ground current through the capacitive coupling due to high capacitance between PV module frame and PV module terminals. There are many inverter structures like H5 inverter by SMA [11], HERIC inverter by Sunways [12], REFU inverter by Refu Solar [13], Full Bridge Inverter with DC Bypass by Ingeteam [14] [15], Full Bridge Zero Voltage Rectifier [16], Conergy NPC inverter by Conergy [17] are proposed to reduce the EMI problem and common mode ground current. But these topologies are suitable for multi string and mini central inverters with power range approximately 20kW. These inverters cannot operate at low switching frequency without trading off with power quality and maximum power point tracking. So, high switching loss cannot be avoided in these inverters. The multi level inverter can effectively reduce the EMI problem, common mode current and device stresses by operating at low switching frequency, without trading off with power quality. Also a multilevel inverter is useful to reduce the cost and size of power filter. Such inverter requires several number of dc power sources depending on the number of level and voltage ratio of dc buses. Multiple power sources can be easily be obtained by dividing the photovoltaic modules in groups. As a result, multilevel inverters are becoming increasingly popular in photovoltaic applications [2-4]. However, there is a lot of challenge to use multilevel inverter in photovoltaic power plants. As the number of level of the inverter increases, the number of device also increases. The challenge of using multilevel inverter in photovoltaic application is to reduce the number of switches without compromising with power quality (Number of levels). This paper proposes a hybrid topology of multilevel inverter to reduce the number of switching devices in the entire converter system. The proposed topology is a hybrid of cascaded H-bridge multilevel inverter (CHBMLI) and neutral point clamped

multilevel inverter (NPCMLI). Asymmetric dc bus voltage ratio is used to increase the number of levels. CHBMLI and NPCMLI topologies are hybridized to improve power distribution ratio of cells: this reduces number of dc-dc converters for maximum power point tracking (MPPT), results reduction of semiconductor devices in overall system and improves the efficiency. Third harmonics is injected to increase the dc bus utilization and to obtain more number of levels in line to line voltage: which will increase power quality/reduce the filter size. Nearest voltage level control modulation technique is used to reduce computational burden.

The paper is organized in six sections. Section-I has explained the importance, motivation and challenges to use multilevel inverter in grid connected photovoltaic systems, and highlights the basic approach of the paper to meet the challenges. Section-II proposes a suitable hybrid multilevel inverter topology to build cost effective, efficient and high power quality inverter, based on various requirements of photovoltaic system. This section also proposes a modulation technique to have reduced switching loss and good dynamic performance, and a method to increase the line to line voltage and number of levels in line-to-line voltage. Section-III describes the implementation detail of MATLAB/Simulink model of the system and its design aspects. Section-IV discusses the simulation results. Section-V discusses about experimental results. Section-VI concludes the work.

II. TOPOLOGY AND MODULATION TECHNIQUE

A. Selection of Topology

A suitable topology is required in order to design efficient grid connected photovoltaic system. The number of switches has to be reduced to reduce the cost and optimize device losses. The number of levels has to be increased to achieve good power quality. Also, higher number of level allows fundamental frequency switching resulting in less switching loss and low electromagnetic interference (EMI). There are three basic topologies of multilevel inverters: Diode clamped multilevel inverter (DCMLI), Cascaded H-bridge multilevel inverter (CHBMLI) and Flying capacitor multilevel inverter (FCMLI). Of these, DCMLI suffers from high device count at higher number of levels, mainly due to large number of clamping diodes. Also this requires special effort to take care of capacitor charge balance. FCMLI also suffers from charge balance problem and large device count. CHBMLI with isolated voltage source connected in each dc bus of the H-bridges is inherently stable against any kind of capacitor unbalance. Also, it is convenient to divide the large number of PV modules of a PV power generation system in small number of sections. This is convenient to obtain isolated dc sources required for CHBMLI topology. But CHBMLI also requires large number of devices if all the H-bridges are connected with equal dc bus voltage. Asymmetric dc bus voltage ratio can help to reduce the number of switching devices to achieve a given level. Also, this allows switching of high-power (at higher dc bus voltage) cell closer to fundamental frequency, with highest power cell (Highest dc bus voltage) in fundamental frequency. This helps to optimize switching losses [5]. Mainly two kinds of asymmetry is reported in literature: binary (where the voltage ratio of CHB cells is V, 2V, 4V … 2^{N-1} V) and trinary (where the voltage ratio of CHB cells is V, 3V, 9V … 3^{N-1} V). In binary voltage ratio, it is possible to achieve any level of voltage within the range by only addition of cell voltages. In trinary voltage ratio, maximum number of level is possible to achieve at the cost of redundancy. As a result, in trinary, it is unavoidable to subtract the voltage of lower voltage cell from the higher voltage to achieve some of the voltage levels within the range. This causes the lower voltage cells to supply a small fraction of total supplied power. In some modulation index it may be observed that the lower voltage cells are absorbing power while overall system is working as inverter [6]. Trinary voltage ratio requires some special circuit/technique to take care/avoid the regeneration problem. Regeneration in lower voltage cells are tackled with circuits or techniques, both of which trades off with power quality, cost and efficiency [7]. So, binary voltage ratio can be used as a solution to avoid regeneration of lower voltage cells. This also helps to improve power distribution ratio. However, the power distribution ratio for a binary voltage ratio is not very good when the number of CHB per phase is greater than three even if it is much better than a trinary voltage ratio. For example, when three H-bridges are cascaded per phase, for a trinary voltage ratio, the power distribution ratio of H-bridges is: **81:14:5** for cells with voltage 9V, 3V and V respectively. While the binary voltage ratio results power distribution ratio **59:28:13** for cells with voltage 4V, 2V and V respectively. This ratio can be further improved. It is possible to integrate equal voltage cells of all phases by using a neutral point clamped (NPC) structure as shown in Fig. 1. It can be noted that the NPC structure must be connected to the neutral point. So, H-bridges with higher voltages are cascaded with NPC structure as shown in Fig. 1. This simply increases the power distribution ratio of lowest voltage cell by three times for a three phase system. Hence, the modified power distribution ratio becomes **47:23:30** for cells with voltage 4V, 2V and V respectively.

The cell with lowest voltage (V) will be common to all three phases with NPC structure as shown in Fig. 1. Integration of small groups of cells reduces the dc bus voltage ripple as the ripple frequency increases. All the above advantages are obtained at the cost of six extra diodes (two diodes per phase) in NPC structure for neutral point clamping purpose. It can be noted that the two sources of NPC structure can be controlled with a single MPPT tracking dc-dc converter.

B. Selection of Modulation Technique

Modulation technique was selected on the basis of following requirements:

1. Excellent dynamic performance.

2. Capability to manage with low computational resources (Simple online computation).
3. Application of fundamental frequency switching to reduce switching loss.

All the available modulation techniques can be categorized in two major parts:

a. Can operate with pulse with modulation PWM technique
b. Can operate with fundamental frequency switching technique.

To increase the efficiency, fundamental frequency switching can be used for the application, which will help to reduce switching losses. This is possible to use with little compromise in power quality if the number of levels are high enough (more than 11). In proposed asymmetric topology shown in Fig. 1, it is possible to achieve 15 levels per phase. Hence, for the proposed topology, it is possible to achieve desired power quality without high frequency switching.

As the grid frequency and voltage are not fixed, it is required to have excellent dynamic performance with available computational resources. Most of the popular modulation techniques like space vector modulation (SVM), selective harmonic elimination (SHE) or the multi carrier PWM involve high computational requirement and/or high frequency switching in order to achieve good dynamic performance. Nearest voltage level control can be used as a solution. This is one of the simplest modulation techniquea for multilevel inverters. This technique can be used without injecting considerable harmonics, when the minimum voltage level per phase is seven [8] or more. As already discussed, the number of voltage levels per phase for proposed topology is 15. Also, this modulation technique involves simple online computation involving only adder and comparator resulting in very less requirement of on-chip computational resources. Hence this modulation technique can be used with proposed topology, without compromising with power quality.

C. Third Harmonic Injection

Third harmonic voltage is injected in phase voltage in order to have further increase in number of levels in line-to-line voltage. The expression of third harmonic injected modulating wave is given by

$$V(t)=V\times[(2]^{N}-1)\times\{1.15\sin(\omega t)+0.19\sin(3\omega t)\} \quad (1)$$

Third harmonic part of the modulating wave gets cancelled out in line to line voltage. As a result, the expression for modulating wave of line to line voltage becomes

$$V_{LL}(t)=\sqrt{3}\times V\times[(2]^{N}-1)\times 1.15\sin(\omega t)$$
$$=2\times V\times[(2]^{N}-1)\times\sin(\omega t) \quad (2)$$

From the above expression it can be noted that the number of voltage levels in line to line voltage will be $[(2]^{N+2}-3)$, while it is $\sqrt{3}\times[(2]^{N}-1)\times 2+1$ without third harmonic injection. So, the number of voltage levels at line to line voltage after third harmonic injection is becoming 29. Third harmonic injection also increases dc bus utilization. This indicates that there is nearly 15% increase in line voltage. Nearest voltage level control with third harmonic injection results dc bus utilization equivalent to SVM technique, without complex algorithm required to implement SVM with such high number of levels.

III. MODELING AND SIMULATION

Two arm IGBT-Diode based cells are used as basic switching cells to form H-bridge as shown in Fig. 2. And two number of single arm IGBT-Diode based cells are connected in series with clamping diodes to form NPC structure as shown in Fig. 3.

Based on the combination of these two basic switching cells, the entire topology is formed as shown in Fig. 1.

Both switching cells of cascaded H-bridge and NPC structure can be operated in four modes:

***Mode 1*:** Q1 and Q4 ON. It can produce a positive voltage across terminals A and B, ideally equivalent to its DC bus voltage.

***Mode 2*:** Q3 and Q2 ON. Negative voltage across terminals A and B, ideally equivalent to its DC bus voltage.

***Mode 3*:** Q1 and Q3 ON (not for NPC structure) or Q2 and Q4 ON. No voltage by getting bypassed.

***Mode 4*:** All switches are OFF. Blocking/Rectifying mode.

A switching table is formed to operate the inverter in various voltage levels as shown in Table-1. In practical application, it has to be ensured that the maximum output voltage of the converter will not exceed the maximum allowable voltage of the photovoltaic modules: which is typically at the range of 1000V.

	Cell 1 (V) (NPC)				*Cell 2 (2V) (CHB-2)*				*Cell 3 (4V) (CHB-1)*			
Level	*Q1*	*Q2*	*Q3*	*Q4*	*Q1*	*Q2*	*Q3*	*Q4*	*Q1*	*Q2*	*Q3*	*Q4*
1(-7V)	0	1	1	0	0	1	1	0	0	1	1	0
2(-6V)	1	0	1	0	0	1	1	0	0	1	1	0
3(-5V)	0	1	1	0	1	0	1	0	0	1	1	0
4(-4V)	1	0	1	0	1	0	1	0	0	1	1	0
5(-3V)	0	1	1	0	0	1	1	0	1	0	1	0
6(-2V)	1	0	1	0	0	1	1	0	1	0	1	0
7(-V)	0	1	1	0	1	0	1	0	1	0	1	0
8(0)	1	0	1	0	1	0	1	0	1	0	1	0
9(V)	1	0	0	1	0	1	0	1	0	1	0	1
10(2V)	0	1	0	1	1	0	0	1	0	1	0	1
11(3V)	1	0	0	1	1	0	0	1	0	1	0	1
12(4V)	0	1	0	1	0	1	0	1	1	0	0	1
13(5V)	1	0	0	1	0	1	0	1	1	0	0	1
14(6V)	0	1	0	1	1	0	0	1	1	0	0	1
15(7V)	1	0	0	1	1	0	0	1	1	0	0	1

Table-1: The switching table of proposed 15 level hybrid multilevel inverter

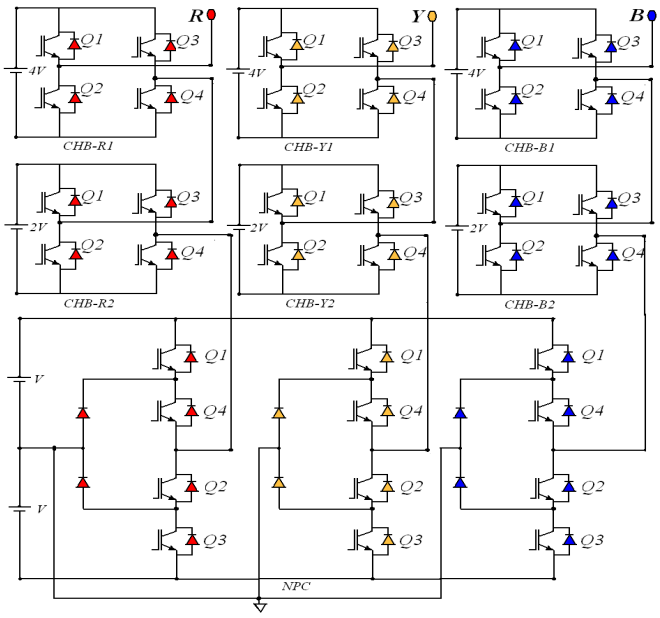

Fig. 1. Proposed NPC-CHB hybrid topology for photovoltaic application

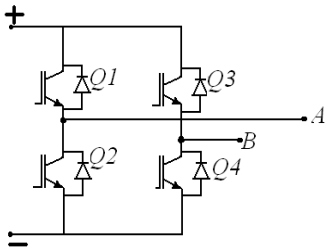

Fig. 2. Basic Switching Cell of Cascaded H-Bridge

So, for this work, it has to be ensured that, the H-bridge cell with lowest dc bus voltage will have maximum dc bus voltage of 140V approximately at maximum possible solar insolation. Grid is simulated with three phase ac source. Line impedance is simulated with R-L series branch. The phase angle of the reference wave of the inverter is controlled for controlling power flow.

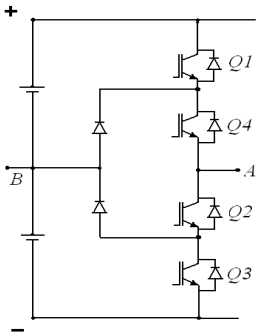

Fig. 3. Basic Switching Cell of Neutral Point Clamped structure

IV. SIMULATION RESULTS AND DISCUSSIONS

Simulation results for the proposed the result is given in following figures. Fig. 4. and Fig. 5. together describes the effect of third harmonic injection. Third harmonic injection makes the phase voltage flat topped as shown in Fig. 4. This results some overlap period between maximum and minimum voltage of two phases: line voltage becomes double the phase voltage. This cannot be achieved without third harmonic injection as shown in Fig.5. It can be observed in Fig. 5, that the number of levels in line voltage is lower than the number of levels at line voltage observed in Fig. 4.

Switching of individual cells of different voltage level of a phase is shown in Fig.6. This individual waves are superposed to form the resultant output phase voltage waveform. The number of switching is highest in cell with lowest voltage, and lowest in cell with highest voltage. If the switching cells are numbered in such a way that, the cell with highest voltage will have lowest number and vice versa, then, the number of switching (turn on and turn off together) per cycle for a switch of a given basic switching cell *C* is:

$$S_n = 2^C - 1 \quad (3)$$

Where, S_n is the switching per cycle for a particular device of a given cell *C*. This can be utilized for the device selection. The power electronic switches available in market does tradeoff between operating frequency, current capacity and voltage rating [9].

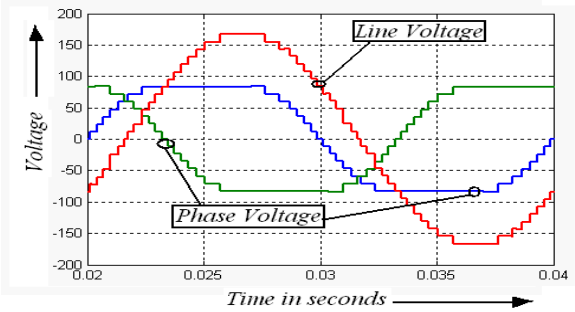

Fig. 4. Line voltage and corresponding third harmonic injected phase voltage

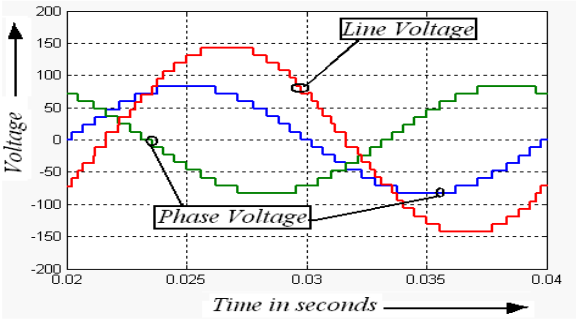

Fig. 5. Line voltage and corresponding phase voltage without third harmonic injection

To realize this topology it is required to use devices with higher-voltage, lower-frequency and devices with lower-voltage higher-frequency. This is convenient for device selection. Overall losses in the devices can be reduced remarkably by proper sizing of device. For medium and high power application, the inverter switching cells with higher voltage and lower frequency may use
GTO/Thyristor and cells with lower voltage may use low frequency (below 5kHz) like Trench-gate/Field-stop IGBT [10]. Grid voltage, corresponding inverter line voltage and line currents are shown in Fig. 7. Total Harmonic Distortion of Line voltage and current are 3.25% and 0.9% respectively. Harmonic contents of the output line voltage are shown in Fig.8. This is much lower than the allowable limit of IEEE 519 standard.

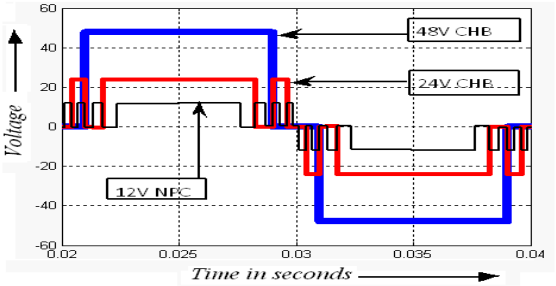

Fig. 6. The voltage waveform of individual basic switching cells of a phase

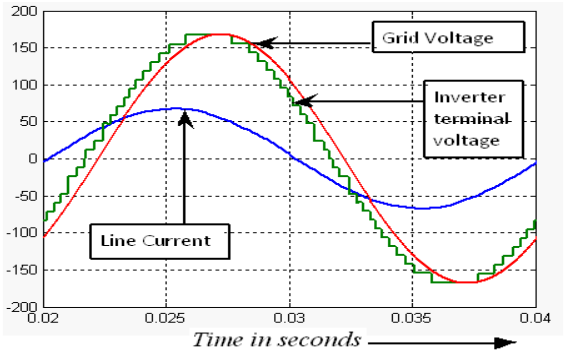

Fig. 7. The line current, line to line inverter output voltage and grid voltage

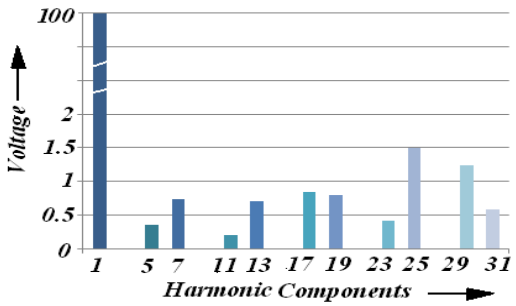

Fig. 8. Harmonic components of output line voltage of the inverter

V. EXPERIMENTAL RESULTS

The hardware setup is under development. The system is operated as a single phase 15 level converter so far. The phase voltage waveform is shown in Fig. 9., which is almost same as simulation result as seen in phase voltage of Fig. 5., except the spikes observed in Fig. 9. This is because of the mismatch of firing time of gate drivers. The duration of those glitches are typically around 10 micro second, as seen in this figure. This short duration glitch will have negligible effect on current harmonic (which is supposed to disappear in line current), all the other components are at least 50 db below fundamental component. The experimental setup is shown in Fig. 11, it can be observed that the dSPACE 1104 is used as controller, and Semikron make IGBTs and gate drivers are used to build the power converters.

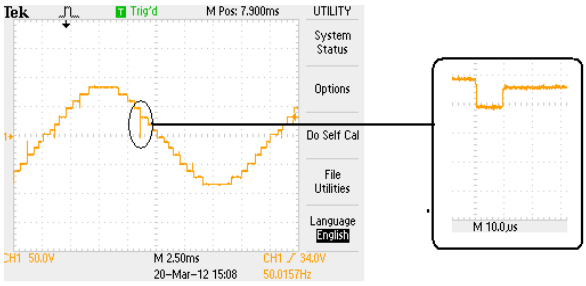

Fig. 9. Output phase voltage of the inverter

Fig. 10. Harmonic components of output phase current of the inverter

Fig. 11. Hardware setup

VI. CONCLUSIONS

A three phase CHB-NPC binary hybrid multilevel inverter topology with simpler and robust modulation technique is simulated in MATLAB/Simulink and partially developed to study its performance in MPPT based grid connected photovoltaic power system application. It was found that the topology and its control technique is competitive to present grid connected photovoltaic central inverter topologies to optimize cost, efficiency and performance.

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