Auto-tuned, Discrete PID Controller for DC-DC Converter for fast transient response

Subhash Chander, *Student Member, IEEE*, Pramod Agarwal, *Member, IEEE* and Indra Gupta

***Abstract*--Ziegler-Nichols tuned PID controller's performances usually are not acceptable for applications requiring precise control. In this paper an improved discrete auto-tuning PID scheme is developed for DC-DC converters where large load changes are expected or the need for fast response time. The algorithm developed in this paper is used for the tuning discrete PID controller to obtain its parameters with a minimum computing complexity and is applied to Synchronous buck converter to improve its performance. To improve the transient response and rise time of the Converter, the controller parameters are continuously modified based on the current process trend. For its implementation a synchronous buck converter is designed and its MATLAB/Simulink model with non-linear parameters is developed and considered. Also, the non-linear effects such as S/H, quantization, delay, and saturation are considered in the close loop model. The simulation results demonstrate the effectiveness of the developed algorithms.**

***Index Terms*--DC-DC Converter, PID Controller, Auto-tuned PID controller, modeling and simulation**

I. Introduction

THE Switch-mode dc–dc converters are power electronic systems that convert one level of electrical voltage into another level by switching action [1]. These converters are very popular because of their high efficiency and smaller size [1]-[2], and therefore are used extensively in personal computers, computer peripherals, communication, medical electronics and adapters of consumer electronic devices to provide different level of dc voltages. The widespread use of switching dc–dc converters in many electronic systems makes a necessity for many electronic system design engineers to design and develop efficient and reliable supplies according to demand.

Switching converters are in general, time-variant, non-linear dynamic systems. The non-linearities arise primarily due to switching, power devices, and passive components, such as inductors, and capacitors. As a result, the conventional linear control techniques can not be directly applied to analyze. To design the feedback compensation using linear control techniques, a dynamic model of the switching converter is needed. The dynamic system should model the low frequency behavior of the system, but should neglect the insignificant behavior at and beyond the switching frequency. Therefore modeling process should involve the approximation to neglect the high frequency phenomena.

The inherent switching operation of power electronic converters results in the circuit components being connected together in periodic changing configurations. They represent different circuit configurations within each switching cycle. Each configuration being described by a separate set of linear state equations. A number of equations must be solved in sequence, for the transient analysis and control design for converters and is therefore difficult. The averaging technique provides a solution to this problem where a single equation may be formed to describe the converter approximately over a number of switching cycles. The filtering action by L-C presents a physical basis for using an average model of the switch, which neglects its switching action while preserving quantitative relationships between average values of voltages and currents at its terminals [2]. The average model provides much faster simulation and control design using MATLAB.

Now-a-days, various advancements in process control techniques has taken place, still PID Controllers have been very popular in closed loop control[3],[4].An extensive survey on the regulatory controllers used in industries reveals that 97% of them are of PID structure, due to their simplicity, applicability and ease of implementations[5].Although many tuning methods have been proposed for PID controllers, but for many of them, performance is quite poor due to among other factors, inadequate tuning of the controller parameters [6],[7].A simple ZN tuning rules is one of most popular method of tuning to obtain reasonable good initial setting of PID Controllers [8] because of familiarity and ease of use [4]. This rule perform satisfactorily for first order system, but they fail to provide acceptable performance for higher order and non-linear systems [7],[8],due to large overshoots and poor load regulation. To overcome such drawbacks several tuning schemes are proposed [7],[8] which are essentially applicable for linear systems. Auto-tuning is the desirable feature for managing difficult tasks in non-linear system control nowadays [4].In a digitally controlled converter, a key advantage is the possibility of auto tuning the controller parameters to adapt to the specific power stage. Efficient, robust and simple implementation of digital controller with embedded tuning capabilities could be a significant breakthrough for digital control in power electronics. The auto tuning process should satisfy two important requirements [9]- Firstly, it should not affect converter operation under nominal condition and secondly, it should be based on a simple and robust algorithm whose complexity should not significantly

Subhash Chander, Pramod Agarwal, and Indra Gupta are with the Department of Electrical Engineering, Indian Institute of Technology, Roorkee-247667INDIA(e-mail:subrag11121@gmail.com,pramgfee@ iitr.ernet.in ,indrafee@ iitr.ernet.in).

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increase the silicon area of the IC controller. Several auto tuning techniques for PID have been available in the literature [10]–[14]. Due to the fact that PID regulators are widely accepted in industrial applications and also the applications of microcontrollers, DSPs and FPGAs have been rapidly increased in power electronics applications, mainly in the medium/high power range [9].However, that most of the existing solutions are too complex for small-power dc–dc converters with integrated digital controllers. Some nonparametric methods for the on-line assessment of system dynamics in dc–dc converters are discussed in [15], [16]; but they requires open-loop operation during the identification process and complex signal processing. The approach presented in [15], [16] has been recently applied to controller auto tuning in [17]. A compressive study has been done [5],[18] and scheme is presented for Ziegler-Nichols tuned PI & PID controller to improve the transient response under set-point change and load disturbances. The proposed controller is tested for a number of higher order linear and non-linear dead time processes.

In this paper general auto-tuning scheme proposed in [5], [18] is adapted for DC-DC converter. A simple auto tuning method for dc–dc converters in which proportional, Integral and derivative gains of the controller are continuously modified based on the current process trend. The purpose of this paper is to implement this scheme to DC-DC converter in discrete form, describing its operation, implementation, simulation performance results and study the performance of converter with load and source variation.

II. Design of Buck Converter

For buck converter of Fig.1 operates in CCM, the relationship between the input voltage (V_i) and the output voltage (V_O) is given as:

$$d = \frac{V_0}{V_i} \tag{1}$$

Where $d=T_{ON}/T_S$ is the duty-cycle, T_S is the switching period and T_{ON} is conducting time of the switch. The boundary condition of CCM and DCM of the buck converter is the critical value of the inductor L_C and is given by [2]:

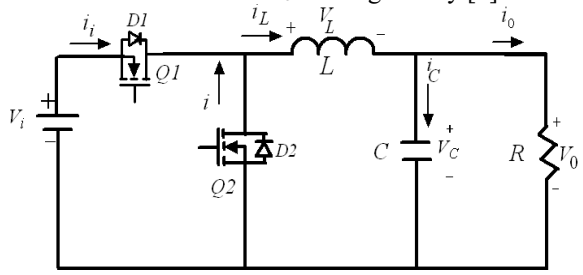


Fig.1 Power stage of synchronous buck converter

$$L_C = (1-d)\frac{R}{2\,f_s} \tag{2}$$

Where, R is the load resistance, and f_s is the switching frequency. The selected inductance should be greater than L_C for CCM [2].However, the inductor value determines the magnitude of ripple current in the output capacitor as well as the load current at which the converter enters discontinuous mode. Normally, a ripple of less than 30% of the average output current is considered for design [19],[20] so as to provide the reasonable efficiency. The value of L can be determined as:

$$d(V_i - V_0) = f_s\, L\, \Delta I \tag{3}$$

The initial choice of the capacitor C is then determined by the allowed voltage ripple ΔV, which is typically 2% of output voltage. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor and is given as [20]:

$$\Delta V = \Delta I\left(\frac{1}{8 f_s C} + ESR\right) \tag{4}$$

However, the output capacitance increases in presence of a load transient requirement [19].The value of capacitance depends on the change in the load, the speed of the loop and the size of the inductor and is given by:

$$C = L\frac{(I_{OH}^2 - I_{OL}^2)}{(V_f^2 - V_i^2)} \tag{5}$$

Where, I_{OH} and I_{OL} is the output current under heavy load and light load conditions respectively. V_f *and* V_i is the final peak and the initial capacitor voltage respectively. The following parameters are considered for design V_i *=5±10% V*, V_{ref}*=2.5V*, *R=1-2Ω, V_0=2.5±2%, I_0=1.25amps,* output ripple of *25 mV (p-p)* at *1.25 amps,* (steady state), output load response of *0.25 V* (load step change from 1.25 to 2.5 amps),*ΔI=0.5* amps (20% of load current),r_c*=2mΩ, r_L=11mΩ,R_{on}=14mΩ, ΔI=20% of I_0 and f_s=195KHz.*The *L=10μH* and *C=47μf* are the determined values for the final design.

III. Modeling of Buck Converter Power Stage

Switching converters after design may be numerically simulated following the system equations. The Simulink requires the system equations of the power stage circuit. These system equations are then used to develop the Simulink model as shown in Fig.3.Fig.4 shows the various sub-systems of the Simulink model of Fig.3.

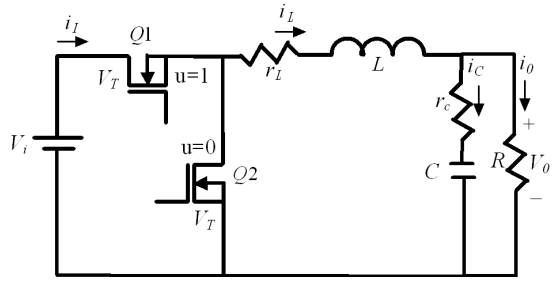


Fig. 2 Buck converter with non-ideal components

The dynamics of this converter operating in CCM, can be understood by using analysis of the circuit shown in Fig.2,and the conduction status of the MOSFET switches *Q1*and *Q2*.The switching action of the switch is described by the switching function *u*, which accepts the values of 0 and 1 [20] and the dynamic equations of converter are written defining the switching intervals [20] .For active switch (*Q1*) conducting:$u_{Q1}=1;u_{Q2}=0$ and for freewheeling switch (*Q2*) conducting:$u_{Q1}=0;\ u_{Q2}=1$.For ideal non-isolated buck converter on-time: $u_{Q1}=u=1$;off-time:$u_{Q2}=\bar{u}=1$.The dynamic and output equations of buck converter are:

$$L\frac{di_L}{dt} = (V_i - V_T)u - V_T\,\bar{u} - i_L r_L - V_0 \tag{6}$$

$$C\frac{dV_c}{dt} = \left(i_L - \frac{V_0}{R}\right) \tag{7}$$

$$V_0 = V_c\left[\frac{R}{R+r_c}\right] + i_L\left[\frac{R\,r_c}{R+r_c}\right] \tag{8}$$

After mathematical manipulation of above equations, the final dynamic and output equations, to develop Simulink model of power stage are given as under:

$$L\frac{di_L}{dt} = (V_i - V_T)u - V_T\,\bar{u} - i_L r_L - V_c\,G_1 - i_L\,G_3 \tag{9}$$

$$C\frac{dV_c}{dt} = i_L G_1 - V_c G_2 \tag{10}$$

$$V_0 = V_c G_1 + i_L G_4 \tag{11}$$

Where, $G_1 = \left[\frac{R}{R+r_c}\right]$, $G_2 = \left[\frac{1}{R+r_c}\right]$, $G_3 = \left[r_L + \frac{R\,r_c}{R+r_c}\right]$

and $G_4 = \left[\frac{R\,r_c}{R+r_c}\right]$ (12)

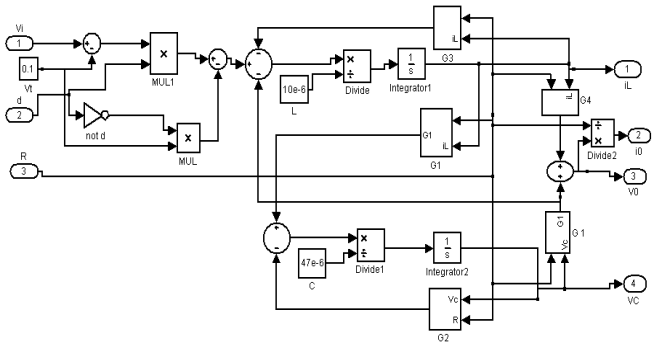


Fig. 3 Simulink Model of buck converter (Power stage)

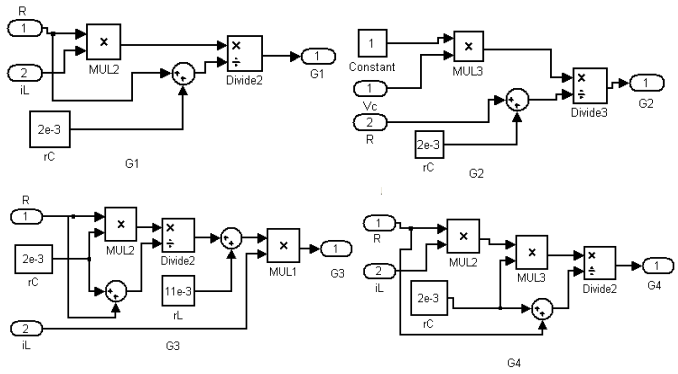


Fig. 4 Simulink models of *G1, G2, G3* and *G4* sub-systems of Fig.3

IV. Closed loop Control System of a DC-DC Converter

Fig.5 shows the closed loop control system of the general DC-DC switching converter with PID-based feedback. The goal here is to minimize the error between V_{Ref} and V_0. As seen in Fig.5, there are four major function blocks: ADC (analog-to-digital conversion), COMPENSATOR (error compensation), DPWM (digital pulse width-modulation) and DC-DC Converter [21]-[23]. ADC is for sampling of analog variable, DPWM is for generating driver signal according to corresponding control laws and COMPENSATOR is for generating the control signal by compensating the error signal the error (V_e).

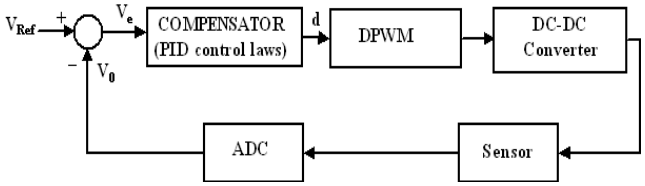


Fig.5 Block diagram of a general PID-based feedback Control of switching converter

The error V_e between the output voltage V_0 and the reference voltage V_{Ref} is $(V_{Ref} - V_0)$ and is processed by COMPENSATOR block with PID compensation algorithm to generate control signal. For the digital control of switching dc-dc converters, PID control can be realized by its compensation block. The control signal will affect the converter characteristics significantly, so it is important to find a suitable compensation way by making good use of digital controller to provide better converter performance. In DC-DC Converters the PID controller is used to compute the duty cycle command corresponding to error V_e, which is applied to DPWM block to generate the switching pulses for the Converter.

V. Discrete PID Control Algorithm

A typical closed loop system using a PID controller is shown in Fig.5.The PID block provides the compensation in the feedback control of the switching converters. The ideal continuous time PID controller can be expressed as:

$$u(t) = K_p\left[e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\frac{d}{dt}e(t)\right] \tag{13}$$

Where *u(t)* is the control output, K_p is constant coefficient of the proportional gain, T_i is integral time or reset time, T_d is the derivative time or rate time and *e* is the error between the reference V_{Ref} and output V_o, the transfer function of corresponding PID controller is given as:

$$u(s) = \left[K_p + \frac{K_i}{s} + K_d.s\right]e(s) \tag{14}$$

Where K_P, $K_i = K_P/T_i$, and $K_d = K_P.T_d$ are the proportional, integral and the derivative gains of the controller, respectively. The continuous-time domain controller of (14) is transformed into the discrete-time domain using the backward difference method .Using this method, (15) the discrete transfer function of a numerical integrator and numerical differentiator are obtained. Then, the discrete PID controller in z-domain is given by (16) The PID structure derived using (17) is shown in Fig (6)

$$s = \frac{z-1}{z.T_s} \tag{15}$$

$$u(z) = \left[K_p + \frac{K_i T_s z}{z-1} + \frac{K_d}{T_s}\frac{z-1}{z}\right]e(z) \tag{16}$$

$$u(z) = \left[K_p + K_i T_s\frac{1}{1-z^{-1}} + \frac{K_d}{T_s}\left(1-z^{-1}\right)\right]e(z) \tag{17}$$

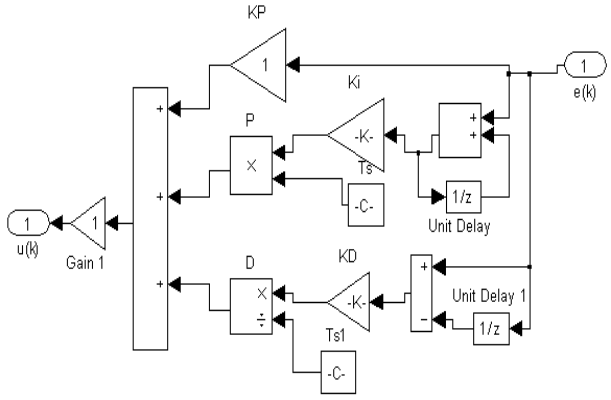


Fig.6 Discrete time PID Controller structure

Similarly, for digital PID control with sampling periods T_s, the following digital PID control algorithm can be obtained by replacing the derivative term and the integral term with abackward difference function and a sum using rectangular integration respectively. The difference equation is given by:

$$u(n) = K_p\left[e(n) + \frac{T_s}{T_i}\sum_{j=0}^{n} e(j) + \frac{T_d}{T_s}\left[e(n) - e(n-1)\right]\right] \quad (18)$$

Where index n and j refer to the time instant. The digital PID block can further be simplified as:

$$u(n) = K_p e(n) + K_i\sum_{j=0}^{n} e(j) + K_d\left[e(n) - e(n-1)\right] \quad (19)$$

Where, $K_i = K_P T_S/T_i$ is the digital integral coefficient, $K_d = K_P T_d/T_S$ is the digital derivative coefficient and K_P is the digital proportional coefficient. To compute the sum, all the past errors have to be stored. This algorithm is called the "position algorithm" [24]

VI. AUTO-TUNED PID CONTROLLER

The simplified block diagram of the proposed PID controller is shown in Fig.7.It shows that the gain updating factor $\beta(k)$ which is a function of converter's error $e(k)$ and the change of error $\Delta e(k)$, continuously adjusts the parameters of the PID controller. So, the starting point of the auto-tuned PID for the buck converter is its corresponding PID. The PID controller parameters are obtained by any standard rules. Since in this paper the PID controller parameters are obtained by ZN tuning rules, which mean that initial settings of the proposed auto-tuned PID controller are based on ZN tuning rules. Each of such ZN tuned parameters i.e proportional, integral and derivative gains of the PID is updated online by a single modifying factor $\beta(k)$ through some relationships. From (19), the difference equation of conventional PID can be derived as:

$$u(k) = K_p e(k) + K_i\sum_{J=0}^{k} e(J) + K_d\,\Delta e(k) \quad (20)$$

Where, $u(k)$ is the control action at K_{th} sampling instant, K_P, K_i and K_d are the proportional, integral and derivative gain respectively. Also, $T_{i,}$ T_d and T_s are the integral, derivative and sampling time respectively.

The K_P, T_i and T_d are calculated according to ZN ultimate cycle tuning rules. The Ziegler-Nichols ultimate-cycle or closed-loop tuning has been widely known as a fairly accurate heuristic method to determine good settings of PID and PI controllers for a wide range of common industrial processes . The Ziegler-Nichols tuning rule is based on the empirical knowledge of the ultimate gain k_u and ultimate period t_u, as shown in Table.1.

Table.1: Ziegler-Nichols tuning formulae

	PID	PI
Proportional gain (K_P)	0.6.Ku	0.45Ku
Integral time (T_i)	0.5.tu	0.85 tu
Derivative time (T_d)	0.125.tu	

For considered synchronous buck converter $e(k)$ and $\Delta e(k)$ are expressed as:

$$e(k) = V_{ref} - V_0(k) \quad (21)$$

$$\Delta e(k) = e(k) - e(k-1) \quad (22)$$

Where V_{ref} is the reference voltage and V_0 output voltage of the converter. The proposed gain updating factor $\beta(k)$ is defined as:

$$\beta(k) = e_N(k).\Delta e_N(k) \quad (23)$$

Here, $e_N(k) = \left[\frac{e(k)}{e_{\max}}\right]$ and $\Delta e_N(k) = \left[e_N(k) - e_N(k-1)\right]$ are the normalized values of $e(k)$ and $\Delta e(k)$ respectively and e_{max} is the maximum possible value of the error. From (23) it may be assumed that the possible variation of β will lie in the range [-1,1] for all closed loop stable operation. In this method K_P, K_i and K_d will be continuously modified by the gain updating factor $\beta(k)$ with the following simple empirical relations:

$$K_p^m(k) = K_p\left(1 + k_1|\beta(k)|\right) \quad (24)$$

$$K_i^m(k) = K_i\left(1 + k_2\beta(k)\right) \quad (25)$$

$$K_d^m(k) = K_d\left(1 + k_3|\beta(k)|\right) \quad (26)$$

Using (14), the transfer function of auto-tuned PID controller is given as:

$$u^{AT}(s) = \left[K_p^m + \frac{K_i^m}{s} + K_d^m.s\right]e(s) \quad (27)$$

Using (15), the corresponding z-domain transfer function of auto-tuned PID controller is given as:

$$u^{AT}(z) = \left[K_p^m(k) + K_i^m(k).T_s\frac{1}{1-z^{-1}} + \frac{K_d^m}{T_s}(k)\left(1 - z^{-1}\right)\right]e(z) \quad (28)$$

Similarly, for digital auto-tuned PID controller, with sampling periods T_s, the difference equation is given by:

$$u^{AT}(k) = \left[K_p^m(k)e(k) + K_i^m(k)\sum_{J=0}^{k} e(j) + K_d^m\left[e(k) - e(k-1)\right]\right] \quad (29)$$

Where, $K_p^m(k), K_i^m(k)$ *and* $K_d^m(k)$ are the modified proportional, integral and derivative gains respectively at k_{th} instant and $u^{AT}(k)$ is the corresponding control action at k_{th} sampling instant .$K_{1,}K_2$ and K_3 are three positive constants, which are used to produce the required variations of $K_p^m(k), K_i^m(k)$ *and* $K_d^m(k)$ from their respective initial values to achieve the desired response. These parameters are properly tuned by choosing the appropriate value of $K_{1,}$ K_2 and

K_3.In present work, the values of K_1, K_2 and K_3 are selected heuristically keeping in mind an overall improved performance of the converter under source and load variations.

The objective of this auto-tuning scheme is that, any change in source voltage or load disturbance, the three parameters $K_p^m(k), K_i^m(k)$ *and* $K_d^m(k)$ will be continuously adjusted by a non-linear updating factor β in order to have a quick recovery of the process during source and load transient without large number of oscillations. Hence it presents the faster dynamic response as verified in the simulation results, by introducing real time non-linear variations for achieving an enhance control performance. Equations (24)&(26) indicate that in auto-tuned both K_p^m *and* K_d^m are increased throughout the entire operating cycle, though, may not be in the same proportion due difference in the values of K_1 and K_3 while the integral gain K_i^m (25) is either increased or decreased from its initial values depending upon the sign of the error.

An important feature of this auto-tuned PID controller is that as the traditional control structure is preserved, an existing conventional PID can be modified into the proposed form by incorporating the easily computable dynamic factor β. Moreover, the proposed scheme is model free since β depends only on the recent process states, normalized error e_N and normalized change in error Δe_N.

VII. Discrete Auto-tuned PID Controller Implementation On synchronous Buck Converter

The initial values of Controller parameter gains are determined using Ziegler-Nichols ultimate sensitivity method .The criteria for adjusting the parameters are based on evaluating the system at the limit of stability rather than on taking a step response. The PID controller parameters for a converter that may or may not include a delay. Briefly, the experimental technique is as follows:

- Place the controller in proportional mode only
- Set K_P as variable, T_i is infinity and the value of T_d is equal to zero.
- K_d is increased from zero to critical value i.e until the closed loop system output goes Marginally stable; record K_d, which is the *ultimate gain* called as K_u and the *ultimate period*, t_u
- The Ziegler-Nichols tuning formulae of table.1 is based on the empirical knowledge of the ultimate gain K_u, and ultimate Period, t_u. These are then used to obtain the tuning parameters of PID controller.

These are the initial values of controller parameters; with trial and error approach the final tuned values for K_p, K_i and K_d are obtained. The discrete PID structure with tuned controller parameters obtained is shown in Fig.6.To determine the z-transfer function of auto-tuned PID controller of (28), the following simple empirical relations are obtained.

$$K_p^m(k) = K_p\left(1 + k_1\left|\beta(k)\right|\right) \tag{30}$$

$$K_i^m(k).T_s = K_i T_s\left(1 + k_2\beta(k)\right) \tag{31}$$

$$\frac{K_d^m(k)}{T_s} = \frac{K_d}{T_s}\left(1 + k_3\left|\beta(k)\right|\right) \tag{32}$$

With tuned parameters, the final empirical relations applicable to synchronous buck converter are given as:

$$K_p^m(k) = 2\left(1 + 2\left|\beta(k)\right|\right) \tag{33}$$

$$K_i^m(k).T_s = 0.41\left(1 + 10\ \beta(k)\right) \tag{34}$$

$$\frac{K_d^m(k)}{T_s} = 9.36\left(1 + 12\left|\beta(k)\right|\right) \tag{35}$$

The simulink model of complete structure of auto-tuned, discrete PID controller is shown in Fig.7 and the modified controller parameters are given in Fig.8

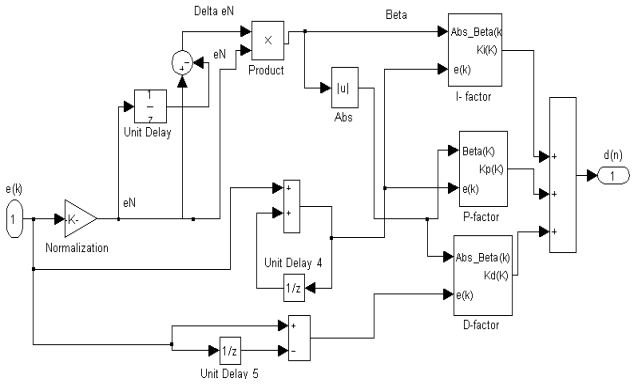
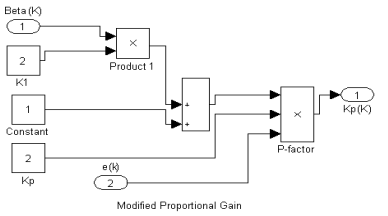
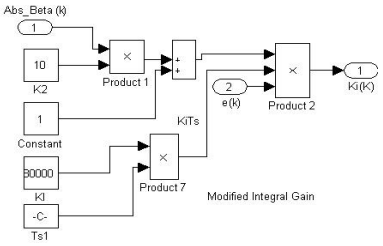


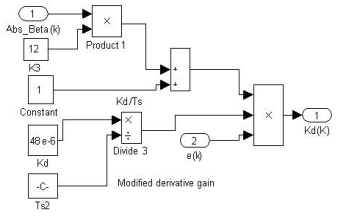
Fig. 7 Auto-tuned PID Controller structure for DC-DC Converter



(a)



(b)



(c)

Fig.8 Modified controller gains (a) Proportional (b) Integral and (c) Derivative

The exact values of modified parameters for considered synchronous buck converter are given by (33), (34) and (35) respectively.

VIII. Simulation Results

A Matlab/Simulink model developed for synchronous buck converter of Fig.1 is shown in Fig.3. It is composed of power

stage modeled in section III, Auto-tuned PID controller designed in section VI and VII, ADC and DPWM models, in addition to the variable load and source voltage. The ADC model consists of an element that performs subtraction of the output voltage value from the reference to generate the error voltage, converter gain, S/H, quantization effects, delay, and saturation blocks. An Auto-tuned PID controller model represented by (28), shown in Fig.7 .The used model is design as explained in section VII . In the considered model, the DPWM generates the pulse signal corresponding to duty command presented by the controller and it has 9-bit resolution. The quantizer, gain block and a duty ratio limiter are included. The variable load and source voltage models are also included in the converter to study the dynamic performances of the converter.

The variable source block and a variable load block to provide V_i=5±10% V and the load transition from *2-1-2*Ω are included in the closed loop simulink model of synchronous buck converter with Auto-tuned PID controller as shown in Fig.9.

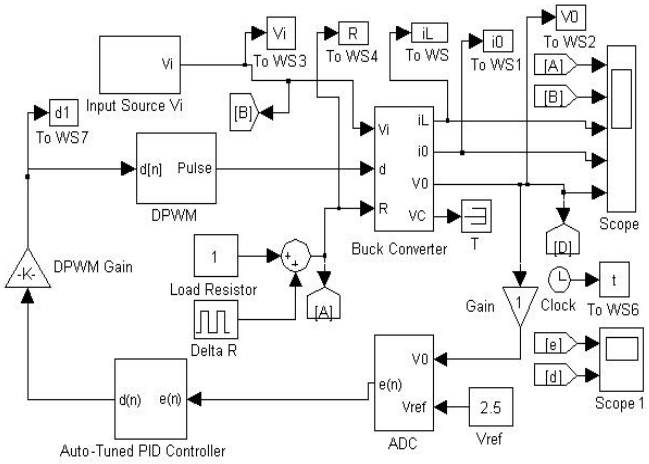


Fig.9 Closed loop Simulink model of synchronous buck converter with Discrete Auto-tuned PID Controller.

The simulation results for, the output current $i_{0,}$ inductor current i_L and output voltage V_0 (with PID), Output voltage V_{01} (with Auto-tuned PID) are shown in Fig.10.

The change in input voltage is shown in Fig.10 (a), the nominal voltage of 5V changes to 5.5V, 5V, 4.5V and back to 5V at 3 ms, 6ms, 9ms and 12ms respectively. The converter has load of 1.25 amps and changes to 2.5 amps and back to 1.25 amps in t= 0, 5ms, 10ms respectively corresponding to R=2-1-2 ohms as shown in Fig 10(b) and 10(d).

As shown in table2,for the input voltage transient, the overshoot and undershoot are around 10% for both PID and Discrete Auto-tuned PID controller, and are around 12% for load transient for 0-100% and 100%-0% (of the nominal load).the rise time of around 0.5ms with Discrete Auto-tuned PID controller as compare to 2.8ms for PID controller. Hence response of the converter is much faster with discrete auto-tuned PID controller. The settling time for input transient is 0.2ms for Auto-tuned PID as compare to 0.8ms with PID. Similarly, settling time for load transient 0.35ms with auto-tuned PID as compare to 0.5ms for PID. Hence, the auto-tuned PID, settle to steady state value faster than PID, after the transient.

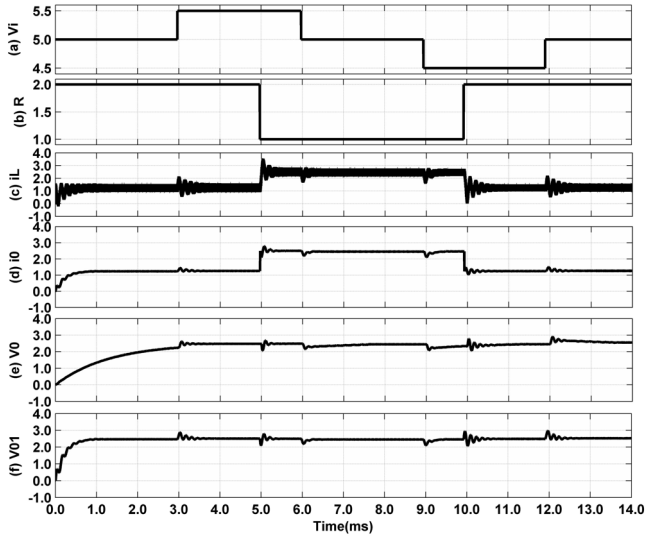


Fig.10 Closed loop response of synchronous buck converter-(a) Input source voltage V_i (b) variation in load resistance (R) (c) Inductor Current (i_L) (d) Load current i_0 (e) output voltage of converter with PID Controller (f) output voltage of converter with Discrete Auto-tuned PID Controller

Table.2. Performance comparison of converter with PID and Auto-PID controllers

Performance parameters	Type of Transient	%	PID	Auto-tuned PID
Transient response	Input transient	Overshoot	10.0	10.0
		Undershoot	10.0	10.0
	Load transient	Overshoot	12.0	12.0
		Undershoot	12.0	12.0
Rise time(ms)	---	---	2.8	0.50
Settling time (ms) after	Input transient	---	0.8	0.20
	Load transient	---	0.5	0.35

Simulation results show that the auto-tuned PID controller presents high dynamic performances as compare to PID .The rise time is faster with 82% reduction and average settling time is reduction of 52% is observed.

IX. CONCLUSION

In this paper, a simple model independent discrete auto-tuned scheme has been presented for DC-DC converter. The proposed scheme continuously adjust the controller gains through some easily interpretable heuristic rules using a single non-linear gain updating parameter β defined on the instantaneous process states. It can be easily applied to an existing controller. The effectiveness of the proposed controller has been tested through simulation experiments on synchronous buck converter. The performance of the converter is compared with when general PID controller is applied with initial parameters. The discrete auto-tuned PID has shown consistently enhanced performance both in transient and steady state conditions.

Moreover, the proposed scheme is model free since gain modifying factor β depends only on the normalized error e_N and normalized change in error $\Delta e_{N.}$ The proposed method can easily be applied to other converter topologies.The scheme can easily be implemented using DSP or FPGA.

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XII. BIOGRAPHIES

Subhash Chander graduated in Electronics and Communication Engineering from National Institute of Technology, Srinagar (J&K) India in 1993. He completed his Post-graduate in Electronics and Communication Engineering from Indian Institute of Technology, Roorkee-India in 2004. He is an Assistant Professor in the Department of Electronics and Communication, Govt. College of Engineering and Technology, Jammu (J&K). Currently, he is pursuing research in the field of DC-DC Converters for low power applications at the Electrical Engineering Department, Indian Institute of Technology Roorkee, India. His fields of interest include Micro-electronics, Low-power VLSI designs and FPGA based design, DC-DC Converters for low power applications.

Pramod Agarwal obtained his Bachelor's degree in Electrical Engineering from University of Roorkee, now Indian Institute of Technology Roorkee (IITR), India. He received his Post-graduate and completed his PhD in Electrical Engineering from IITR in 1985 & 1995 respectively. He was a Postdoctoral Fellow with the University of Quebec, Montreal, QC, Canada, from 1999 to 2000. Currently, he is a Professor in the Department of Electrical Engineering, IITR. His fields of interest include electrical machines, power electronics, power quality, FPGA based design, microcontroller, microprocessors and microprocessor-controlled drives, active power filters, multilevel converters, and application of dSPACE for the control of power converters.

Indra Gupta obtained his Bachelor's degree in Electrical Engineering from HBTI Kanpur, in 1984 He received his Post-graduate and completed his PhD in Electrical Engineering from University of Roorkee now Indian Institute of Technology Roorkee, India in 1986 & 1996 respectively. Currently, he is a Associate Professor in the Department of Electrical Engineering, IITR. His fields of interest include simulation, Process Control applications, Microprocessor applications, ANN, Online Control applications and FPGA based Design.