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# Current transformer saturation compensation based on a partial nonlinear model

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ABSTRACT

This paper proposes a partial nonlinear model to accurately represent the nonlinear saturation characteristic of a current transformer (CT). Based on the model, the saturated section of the secondary current as well as the unsaturated section can be used in a regression process to estimate model parameters. The saturated section normally lies near the inception of a fault, therefore accurate parameters can be obtained faster compared with the methods using only unsaturated sections. The pre-fault remanent flux and DC-offset, which could significantly influence CT saturation, are both considered in the model, thus they do not affect the accuracy of the parameter estimation. The computational load of the regression calculation is significantly reduced by using separable nonlinear least squares (SNLLS) method. This provides the feasibility to implement the method for real-time protective relaying. The performance of the method has been evaluated on the data obtained from both PSCAD/EMTDC simulation and live recording with a test CT. The method has also been implemented in a Field Programmable Gate Array (FPGA).



## 1. Introduction

Iron-core current transformers (CTs) are widely used for current measurements in power systems due to their reliability and acceptable cost. Their major disadvantage is concerned with the saturation of the iron-cores, which causes the distortion of secondary currents appearing at the inputs of protection relays [1]. This may, in consequence, lead protection relays to malfunction. Two ways are normally used to alleviate this impact: (1) using large iron-core CTs to reduces the probability of the occurrence of CT saturation; (2) employing compensation algorithms to eliminate the influence of CT saturation. Obviously the latter is more economical.

In recent years, the techniques of compensating the secondary current distortion caused by CT saturation have been intensively studied. In [2], the magnetizing current of a saturated CT is estimated by applying the calculated instantaneous flux of the CT to the magnetization curve of the CT. This technique relies on the assumption that the remanent flux in the CT is zero prior to the fault, which has the drawback that the assumption cannot be guaranteed in every fault condition. In [3,4], the remanent flux problem is avoided by detecting the exact start points of the distorted secondary currents using difference functions and a morphological lifting scheme (MLS) respectively. The instantaneous flux at these points is equal to the flux at the knee point in the magnetization curve of the CT. However, due to the disturbances caused by anti-aliasing filters and noise, the start points detected by these methods may have large deviations from their true values. Some methods use a complex inverse function to get the compensated current with the saturated current as input [5,6]. Usually, an artificial neural network (ANN) is used as the complex inverse function. Theoretically, ANN can provide satisfactory compensation. However, it has to be trained with comprehensive data, which cover all the possible saturation scenarios of the CTs. Without these data and sufficient training, the accuracy of the ANN approach would not be ensured. Another group of methods apply a linear regression [7] and a discrete dynamic filter [8] on the unsaturated sections of the secondary current to reconstruct the compensated current. They utilize wavelet and a threshold criteria respectively, to extract unsaturated sections from a distorted secondary current. Using these methods, sufficient length of unsaturated sections is required to obtain accurate results. If the methods are used to deal with a severely saturated current, which has only a very short unsaturated section in each fundamental cycle, more than one cycle of the current is needed to get enough unsaturated sections.

In [9] the authors has proposed a novel method which can compensate CT saturation current accurately and rapidly. In this paper, the method has been further developed, thoroughly verified and implemented in a Field Programmable Gate Array (FPGA) based embedded system. Based on a partial nonlinear model, both unsaturated and saturated sections of a distorted secondary current are used by the method to conduct a nonlinear regression, therefore only a short section of current waveform is required to achieve an

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Fig. 2. Sample power system model.

problem by assuming $a_5$ is known. Accordingly, its analytical solution is

$$a_{(1\text{–}4)} = L^{+}(i_s + F_{im}(a_5)), \quad (12)$$

where $L^{+}$ is the Moore–Penrose generalized inverse of L and can be calculated by $L^{+} = (L^{T}L)^{-1}L^{T}$. Then, by replacing $a_{(1\text{–}4)}$ in (10) with (12), a one-dimension NLLS problem is formed as

$$r_{SNLLS}(a_5) = f_{SNLLS}(a_5)^{T} f_{SNLLS}(a_5), \quad (13)$$

where

$$f_{SNLLS}(a_5) = (I - LL^{+})(i_s + F_{im}(a_5)). \quad (14)$$

Once $a_5$ is obtained, $a_{(1\text{–}4)}$ can be calculated by applying it back to (12). The amplitude and the relative phase of the fundamental waveform of the fault current can also be directly calculated from $\sqrt{a_1^2 + a_2^2}$ and $\arctan(a_2/a_1)$, respectively.

The NLLS problems described in (11) and (13) are solved by using two widely adopted NLLS solving methods, Powell-s Dogleg trust-region method [12] and Levenberg–Marquardt (LM) method [13]. Test results have shown that the convergence speed of the two methods increases around by 50 percent when SNLLS method is applied, and generally Dogleg trust-region method performs better than LM method under the same conditions.

According to the analysis of the pro"le of the one-dimension objective function $r_{SNLLS}(a_5)$, which is shown in Fig. 3. It is a non-convex function. It is well understood that when solving non-convex functions, the performance of Quasi-Newton NLLS solvers (e.g., LM method, Dogleg method) is affected by the initial points of the iterations. To guarantee always "nding the globe minimum of $r_{SNLLS}(a_5)$ (i.e. convergence), the initial points are set to be equal to positive or negative maximum possible core "ux of the CT according to the polarity of the saturation. A simple MLS based method introduced in [4] is applied to determine the existence of CT saturation and its polarity.

## 4. Performance evaluation

To evaluate the performance of the proposed method, a wide range of test cases were established and analyzed. The test cases are divided into two groups with respect to the sources of test data: (a) the simulation data generated form PSCAD/EMTDC, and (b) the real data live recorded from a test CT. The real data are provided by courtesy of Siemens Protection Devices Ltd. In the following description, all of the quantities are referred to the secondary side. The sampling rate is 32 points per cycle. To measure the compensation accuracy

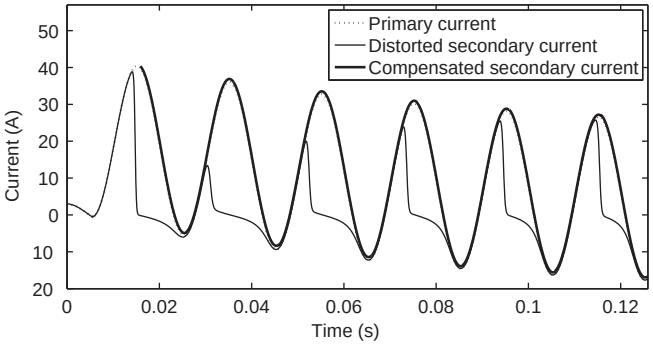


Fig. 4. Compensated result of case 1.

of the test cases in the following sections, a normalized root mean square error $_{NRMS}$ is de"ned as

$$_{NRMS}\% = \frac{\sqrt{(1/N)\sum_{n=1}^{N}(i_p(n) - i_{cs}(n))^2}}{\max(i_p) - \min(i_p)} \times 100, \quad (15)$$

where $i_{cs}$ is a compensated secondary current.

### 4.1. Test cases with simulation data

A sample power system model, as shown in Fig. 2, is built in PSCAD to generate test data. The model consists of two sources and a single transmission line. S1 and S2 are equivalent AC voltage sources whose phase-to-phase voltages are both 220 kV but with different phase angles. $Z_{S1}$ and $Z_{S2}$ are equivalent impedances of S1 and S2. The length of the transmission line is 300 km. Single phase to ground faults are put on the line. To cover all possible operation conditions, various parameters are used, including fault locations (10–150 km), fault inception angles (0–315 ), X/R ratio (10–60) and fault resistance (0.1–5 ). The CT model used in the simulation is based on Jiles–Atherton theory [14]. Its settings are: ratio (1000:5), secondary resistance (0.5 ) and secondary inductance ($0.8 \times 10^{-3}$ H). A pure resistive or 0.5 power factor (pf) burden is connected to the secondary side. The remanent "ux is set to be in the range of -80% to 80% of the saturation "ux of the CT.

In total, 274 simulation data sets have been generated using the model. A consecutive window of a half cycle is applied in the compensation calculation. The average and maximum $_{NRMS}$ of these tests is 1.03% and 5.12%, respectively. To illustrate the performance of the proposed method, "ve representative test cases, which cover typical fault scenarios, are presented below. The con"gurations of these "ve cases are given in Table 1.

1) Case1: normal saturation scenario

Case 1 represents a normal saturation scenario. Fig. 4 shows the compensated result. The bold line is the reconstructed secondary current, which is an accurate approximation of the primary current. It also shows that the valid output of the

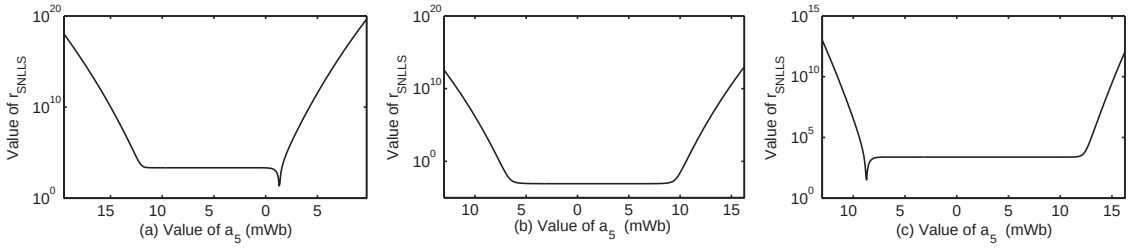


Fig. 3. Pro"les of $r_{SNLLS}(a_5)$ under different condition. (a) Saturation with positive polarity and no remanent "ux. (b) No saturation. (c) Saturation with negative polarity and -80% remanent "ux (i.e., the remanent "ux is 80% of the "ux at the CT saturation point with negative polarity).

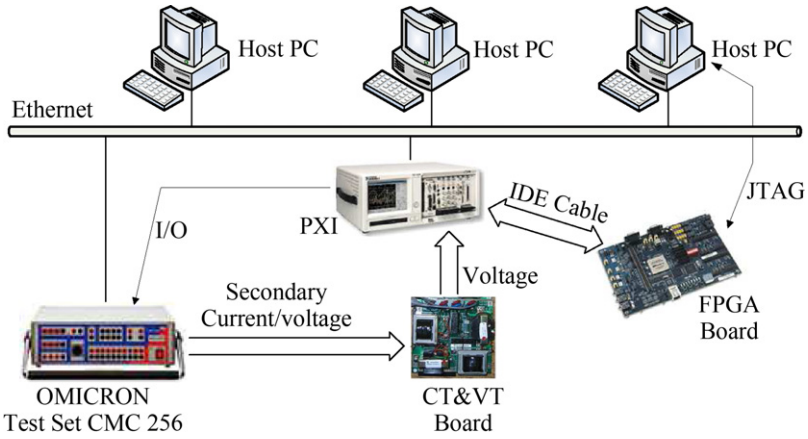


**Fig. 13.** Hardware structure of the test bench.

(1) a large dynamic range of numbers is required by the SNLLS method, which is difficult to be implemented using fixed-point arithmetic; (2) floating-point elements consume much more FPGA resources than their fixed-point counterparts, therefore element sharing must be applied to reduce resource usage; (3) the complexity of the SNLLS method and the piped lined structures of floating-point elements make the method difficult to be implemented in a fully fixed logic module, thus an FPU is a suitable choice. This FPU has seven paralleled calculation channels and supports some acceleration functions for vector-based calculations. The whole SoC based protection relay is implemented on an Altera DSP Development Board, Stratix II Edition. The performance and resource usage of the compensator module in the FPGA chip are given in Table 3. With an execution frequency of 120 MHz and a 32 points per cycle sampling rate, the calculation can be completed within 0.826 ms. This calculation time is slightly longer than a sampling interval (0.625 ms). However as the consecutive window is employed by the compensator, this calculation time does not cause problems in the real-time implementation. Moreover, the calculation time can be further reduced by using a faster FPGA chip.

### 5.2. Real-time test

To test the real-time performance of the SoC based protection relay, a real-time protection relay test bench has been established. Its major components and their connections are illustrated in Fig. 13. During the test process, the simulated and live recorded secondary currents are played back by the OMICRON 256 Test Set. These currents are converted to low voltage signals (−5 to +5 V) through a CT board, and then digitized by an IO module in the PXI system, which is an modularized industrial machine running a LabVIEW real-time operating system. The digital samples are transferred to the FPGA board and are processed by the SoC based protection relay implemented inside the FPGA chip of the board. The processed results are sent back to the PXI system and can be observed in real-time through a host PC which displays a remote interface of the PXI system. A screen snapshot of one compensation test is given in Fig. 14. The white and red lines are a saturated current and its compensated current respectively. Because the communication channels between the PXI system and the FPGA board can only support fixed-point data, the amplitude of these currents is in a fixed-point format. As shown in the figure, an accurate compensated output is available after a delay of 0.8 cycle.

**Table 3**
Performance and resource usage of the FPU module.

| | Number of usage | Percentage of total resource |
|---|---|---|
| Adaptive look-up tables | 2359 | 4.88% |
| Memory bits | 316,027 | 12.42% |
| 18 × 18 multipliers | 36 | 25% |
| Maximum frequency ($F_{MAX}$) | 120.26 MHz | n/a |

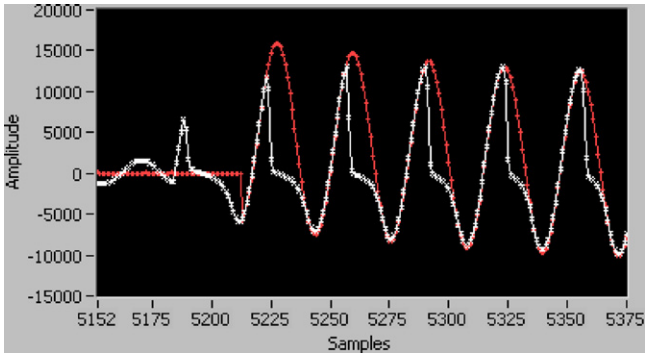


**Fig. 14.** A snapshot of a compensation test using the test bench.

## 6. Conclusion

This paper presents a promising method for CT saturation compensation. This method obtains accurate parameters faster than the linear regression methods. The fundamental amplitude and phase of the secondary fault current can also be directly obtained from the estimated parameters, which may be used in over-current relays and distance relays to remove the disturbance caused by CT saturation and exponentially decaying DC-offsets. The computational load of the nonlinear regression decreases greatly by applying the SNLLS method. The proposed method has been fully tested with data obtained from both simulation and live recording. It has also been implemented in an FPGA chip and tested in a real-time environment. The test results show the method is capable of providing a reliable input signals to power system protection devices.

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