Phase-Shift Controlled Isolated Buck-Boost Converter with Active-Clamped
Three-Level Rectifier (AC-TLR) Featuring Soft-Switching within Wide Operation Range

Hongfei Wu, Member, IEEE, Yangjun Lu, Kai Sun, Member, IEEE, Yan Xing, Member, IEEE

Abstract—An active-clamped three-level rectifier (AC-TLR) is derived from the diode-clamped three-level inverter, by replacing the active switches and the diodes in the three-level inverter with the diodes and active switches, respectively. Novel isolated Buck-Boost converters, featuring single-stage conversion and soft-switching within wide operation range, are developed based on the proposed AC-TLR. By utilizing the AC-TLR, the voltage stress on the power devices and passive components, including the rectifying diodes, the active-clamping switches, the flying capacitor and output filter capacitors, is reduced to the half of the output voltage. Low voltage rating switching devices with better switching and conduction performances, and a transformer with reduced turns ratio and parasitic parameters are used to enhance the efficiency. The full-bridge isolated Buck-Boost converter with the proposed AC-TLR is analyzed in detail as an example. An optimized phase-shift control strategy is employed to realize isolated Buck and Boost conversion. Soft-switching of all of the switching devices in both the primary and secondary-side circuits is achieved within the whole operation range by using the proposed AC-TLR and the phase-shift control strategy. Experimental results on a prototype with 380V output verify the effectiveness of the proposed AC-TLR and its derived isolated Buck-Boost converters.

Index Terms—DC-DC converter, three-level rectifier, isolated Buck-Boost converter, soft-switching, phase-shift control

I. INTRODUCTION

Isolated DC-DC converters have been widely used for the applications in which the input voltage is much lower or much higher than the output voltage, or in which galvanic isolation is required, for example, the battery-sourced front-end converters for uninterruptible power supplies (UPS) and stand-alone renewable power systems [1], battery chargers for electric vehicles [2][3], and the maximum power point tracking (MPPT) converter for renewable power generation systems [4]. The isolated converters can be classified into three categories: Buck converters [3], Boost converters [4] and Buck-Boost converters [5][6]. Generally, the conversion efficiency of Buck converters decreases as the voltage conversion ratio decreases, and the efficiency of Boost converters is found to decrease as the voltage conversion ratio increases. It is very important to achieve high efficiency power conversion within a wide voltage range, especially for the power systems fed by renewable energy and batteries [7][8]. An isolated Buck-Boost converter (IBB) can operate either as a Buck converter or as a Boost converter, it is more flexible in terms of conversion efficiency and voltage range.

For the isolated step-down and step-up applications, many isolated Buck and Boost topologies have been proposed. However, few works on IBB DC-DC converter topologies have been reported in literatures. Most of the IBB converters root in the non-isolated converters. For example, the flyback converter is the isolated version of non-isolated Buck/Boost converter [9]. Likewise, isolated Cuk [10], Sepic [11] and Zeta [12] converters can be derived by inserting a transformer into the original non-isolated Cuk, Sepic and Zeta converters, respectively. However, the efficiencies of these single-switch IBB converters are still low because of the high voltage/current stress on the components and the hard-switching of active switches and rectifying diodes. In addition to the low conversion efficiency and high stress, these single-switch IBB converters can only be used for low power applications. A family of IBB converters is proposed in [5] based on the non-isolated two-switch Buck-Boost converter [13][14]. These IBB converters are built with cascading connection of isolated Buck converters and non-isolated Boost converters. They have the advantages of isolated Buck and Boost conversion, wide voltage gain range and flexible control. However, the power has to be processed through the cascaded two-stage architecture, which lowers the conversion efficiency. On the other hand, the voltage stress of the devices on the secondary-side is much higher than the output voltage. The efficiency is further reduced due to the hard-switching operation of the rectifying diodes and active switches. The semi-dual-active-bridge (SDAB) converters presented in [15]-[18], which are the simplified versions of dual-active-bridge (DAB) converters[19]-[21], can be good options for IBB power conversion. In comparison with the DAB converter, topology and control of

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the SDAB converters are simpler and soft-switching operation range is extended. However, some drawbacks for these SDAB converters are presented in [15]-[18]: (1) Soft-switching performance will be lost for the active switches and diodes in the semi-active-bridge if the normalized voltage gain is less than 1.0 and the converters work in the continuous current mode (CCM) II; (2) The voltage stress on the MOSFETs in the semi-active-bridge is up to the output voltage, which makes them unsuitable for high output voltage applications; (3) The current flows through the body diodes of the MOSFETs in the semi-active-bridge, which leads to severe reverse-recovery problem when the MOSFETs are hard-switching due to the poor characteristics of body-diodes. This problem becomes worse as the output voltage increases. It should be noticed that the output voltages of all SDAB converters in [15]-[18] are lower than 300V.

For high output voltage applications, the reduction of the voltage stress on rectifying devices, especially on the active switching devices such as MOSFETs, is very important for efficiency improvement, because both the conduction losses and switching losses increase significantly as the voltage-rating increases. Low voltage stress on the rectifying devices can be achieved by employing a capacitive output filter, because the voltage of the rectifying devices can be clamped directly by the filter capacitor. There are many kinds of rectification circuits with capacitive filters, such as the center-tapped rectifier, the full-bridge rectifier and the voltage doubler rectifier [22][23]. A voltage doubler rectifier is suitable for high voltage applications, because its output voltage is twice that of the transformer secondary winding, and hence, the turns ratio of the transformer can be reduced. However, the voltage stress of the rectifying diodes in the voltage doubler rectifier is still high as the output voltage. There is a straightforward relationship between an inverter circuit and a rectification circuit, which means a rectification circuit can be derived directly by replacing the active switches in the corresponding inverter circuit with diodes, and vice versa. Two examples are shown in Fig. 1. It can be seen that the rectification circuit corresponding to the full-bridge inverter is the voltage doubler rectifier, as shown in Fig. 1(a), and the corresponding rectification circuit of the half-bridge inverter is the voltage doubler rectifier as given in Fig. 1(b).

The major contribution of this paper is to propose a novel active-clamped three-level rectifier (AC-TLR) based on the diode-clamped three-level inverter topology. Novel IBB converters are harvested based on the proposed AC-TLR as well. Single-stage power conversion, low voltage stress, and soft-switching operation over the whole operation range can be achieved in the proposed converters by adopting the optimized phase-shift control strategy. This paper is organized as follows. In section II, the AC-TLR and its derived IBB converters are presented. In section III, the operational principles of a full-bridge IBB converter are analyzed in detail. The performance of this converter is analyzed in section IV, and experimental results are presented in section V. Finally, section VI concludes the paper.

II. DERIVATION OF THE AC-TLR AND IBB CONVERTERS

A. Derivation of the AC-TLR

There is a straightforward relationship between an inverter circuit and a rectification circuit. A rectification circuit can be derived by replacing the active switches in an inverter circuit with diodes, and vice versa. Two examples are shown in Fig. 1. It can be seen that the rectification circuit corresponding to the full-bridge inverter is the full-bridge rectifier, as shown in Fig. 1(a), and the corresponding rectification circuit of the half-bridge inverter is the voltage doubler rectifier as given in Fig. 1(b).

The AC-TLR-based IBB converters can be constructed based on the proposed AC-TLR. For the primary side of the derived AC-TLR-based isolated converters, the voltage-fed push-pull, half-bridge, full-bridge, three-level input stages and other advanced input stages can be used. Since the AC-TLR has a capacitive output filter, a high-frequency current source should be used as the input of the AC-TLR. In practice, the
III. OPERATIONAL PRINCIPLES OF THE PROPOSED FULL-BRIDGE ISOLATED BUCK-BOOST CONVERTER

The main focus of this paper is the AC-TLR. The input stage can be selected according to different applications. The AC-TLR-based fullbridge IBB (FB-IBB) converter shown in Fig. 3(a) is taken as an example for analysis. The topology of the FB-IBB converter is illustrated in Fig. 4, N is the secondary to primary turns ratio of the transformer. The square wave voltage produced by the primary-side full-bridge inverter is indicated as \( v_p \) in Fig. 4, while the square voltage waveform produced by the AC-TLR is indicated as \( v_s \).

For simplicity, the normalized voltage gain \( G \) is defined as follows:

\[
G = \frac{V_o}{2NV_n}
\]  

The converter operates in the Boost mode when \( G \geq 1 \), and operates in the Buck mode when \( G < 1 \). All of the six active switches, \( S_1 ~ S_6 \), on the primary and secondary sides have a constant duty cycle of 0.5. The switch pairs \( S_1 \) and \( S_2 \), \( S_3 \) and \( S_4 \), and \( S_5 \) and \( S_6 \) are driven complementary, respectively.

The primary-side phase shift angle \( \varphi_P \) is defined to be the phase difference between the gating signals of \( S_1 \) and \( S_5 \), and the secondary-side phase shift angle \( \varphi_S \) is defined to be the phase difference between the gating signals of \( S_3 \) and \( S_4 \). Because the primary and secondary-side phase shift angles serve the same function as the duty cycles of the Buck and Boost converters, respectively, the equivalent primary and secondary-side duty cycles are defined to simplify the analysis,

\[
\begin{align*}
D_p &= \frac{\varphi_P}{\pi} \\
D_s &= \frac{\varphi_S}{\pi}
\end{align*}
\]  

To achieve soft switching and improve the conversion efficiency, an optimized phase-shift control strategy is developed for the FB-IBB converter. To simplify the analysis, the parasitic capacitance of MOSFET is ignored and the transformer is assumed to be ideal.

A. Boost Mode Operating

In the Boost mode, the primary-side duty-cycle \( D_p \) should be maximized with \( \varphi_P = 1 \), and the secondary-side duty-cycle \( D_s \) is used to regulate the output voltage and power, which is similar to the non-isolated two-switch buck-boost converter [13][14]. According to the waveforms of the inductor current \( i_L \), there are two possible operating modes, continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

1) Boost-CCM Mode

Fig. 5 shows the waveforms of the FB-IBB converter in the Boost-CCM mode, where \( T_s \) is the switching period. From the waveform of \( v_s \) in Fig. 5, it is obviously that three voltage-levels, positive-level, zero-level, and negative-level, have been produced by the AC-TLR. There are ten switching stages in one switching period. Due to the symmetry of the circuit, only five stages are analyzed here and corresponding equivalent circuits for each stage are shown in Fig. 6.
Stage 1[t₀, t₁] [Fig. 6(a)]: Before t₀, the switches \( S_2, S_1 \) and \( S_3 \), and diodes \( D_3 \) and \( D_2 \) are ON. The inductor current \( i_{Lf} \) is negative \( i_{Lf}<0 \). The input source \( V_{in} \) and the energy stored in the inductor \( L_f \) are delivered to the output capacitor \( C_{o2} \). Capacitors \( C_{o2} \) is charged, whereas \( C_{o1} \) is discharged. At \( t₀ \), \( S_2 \) and \( S_3 \) are turned OFF. The body-diodes of the switches \( S_1 \) and \( S_3 \) begin to conduct due to the energy stored in \( L_f \). In this stage, the inductor current \( i_{Lf} \) can be calculated as follows,

\[
i_{Lf}(t) = \frac{NV_{in} - V_L}{L_f} (t-t_0) + i_{Lf}(t_0)
\]

Stage 2[t₁, t₂] [Fig. 6(b)]: At \( t₁ \), the switches \( S_1 \) and \( S_4 \) are turned ON with zero voltage switching (ZVS). This stage ends when \( i_{Lf} \) returns to zero. Because the current slope is limited by the inductor \( L_f \), the diodes \( D_3 \) and \( D_4 \) are OFF naturally with zero current and without reverse-recovery loss.

Stage 3[t₂, t₃] [Fig. 6(c)]: At \( t₂ \), \( i_{Lf} \) returns to zero. Because both the \( S_1 \) and \( S_4 \) are ON, the primary-side circuit produce a positive voltage \( V_P \) and applies on the transformer winding. The diode \( D_4 \) begins to conduct due to the ON-state of the switch \( S_3 \), which results in a zero voltage-level \( V_0 \). So the inductor \( L_f \) is charged by the input voltage, which is similar to the operation of a conventional Boost converter. During this stage, the inductor current \( i_{Lf} \) is given as follows:

\[
i_{Lf}(t) = \frac{NV_{in} - V_L}{L_f} (t-t_1)
\]

Stage 4[t₃, t₄] [Fig. 6(d)]: At \( t₃ \), the switch \( S_1 \) turns OFF. Since the current \( i_{Lf} \) is positive, the diode \( D_1 \) begins to conduct. Hence, the input source and the energy stored in the inductor \( L_f \) are delivered to the load. In this stage, the capacitor \( C_{o1} \) is charged, while \( C_{o2} \) is discharged. The inductor current \( i_{Lf} \) is calculated as follows,

\[
i_{Lf}(t) = \frac{NV_{in} - V_L}{L_f} (t-t_3) + i_{Lf}(t_3)
\]

It should be noted that, once \( D_1 \) and \( D_2 \) are ON, the drain-source voltage of the switch \( S_6 \) is clamped to zero, because the voltage of the flying capacitor is equal to the voltage of output dividing capacitor \( C_{o1} \).

Stage 5[t₄, t₅] [Fig. 6(e)]: At \( t₄ \), the switch \( S_6 \) turns ON with
Similar operation is conducted in the remaining stages of the switching period. It can be seen that ZVS can be achieved for all the active switches, while zero-current-switching (ZCS) can be achieved for all the rectifying diodes in the Boost-CCM mode.

2) Boost-DCM Mode

If the inductor current $i_{Lf}$ has decreased to zero before the primary-side switches commutate, the converter enters the Boost-DCM mode. Fig. 7 shows the waveforms of the FB-IBB converter in the Boost-DCM mode. There are five switching stages in half of the switching cycles as well.

Stage 1 [$t_0, t_1$] [Fig. 8(a)]: Before $t_1$, $i_{Lf}$ decreases to zero. So, even though the switches $S_2$, $S_3$ and $S_5$ are ON, there is no power transferred between the primary and secondary sides.

Stage 2 [$t_1, t_2$]: At $t_2$, $S_1$ and $S_3$ are turned OFF.

Stage 3 [$t_2, t_3$] and Stage 4 [$t_3, t_4$]: At $t_2$, $S_1$ and $S_2$ are turned ON with ZCS. The operating principle of this state is the same as that of State 3 in the Boost-CCM mode, whereas the operating principles of Stage 3 and Stage 4 of the Boost-DCM mode are the same as that of the State 4 and Stage 5, respectively, in the Boost-CCM mode.

Stage 5 [$t_4, t_5$] [Fig. 8(b)]: At $t_4$, $i_{Lf}$ reaches zero, and is kept at zero in this stage. Thus, there is no energy transferred between the input and output.

Similar operation is conducted in the rest stages of the switching period. It can be seen that ZCS can be achieved for the primary-side switches and the rectifying diodes, while ZVS can be achieved for all the active switches.

B. Buck Mode Operation

Once the normalized voltage gain is less than one, $G<1$, the converter works in the Buck mode. According to the waveform of the inductor current $i_{Lo}$, the converter can work in either the CCM mode or the DCM mode.

1) Buck-CCM Mode

In the Buck-CCM mode, to overcome the disadvantage of hard-switching of previous SDAB converters with only secondary-side phase-shift control, an optimized duty-cycle equal to the normalized voltage gain $G$ is applied on the
The power flow is controlled by regulating the secondary-side duty cycle $D_S$. Fig. 9 shows the waveforms of the FB-IBB converter in the Buck-CCM mode. There are seven switching stages in half of a switching cycle, and corresponding equivalent circuits for each stage are shown in Fig. 10.

Stage 1 [$[t_0, t_1]$: Before $t_0$, the switches $S_2$, $S_3$, $S_5$, and diodes $D_3$, $D_4$ are ON, and the inductor current $i_{L_f}$ is zero. The input source and the energy stored in the inductor $L_f$ are delivered to the load. The output capacitor $C_{o2}$ is charged, whereas $C_{o1}$ is discharged. At $t_0$, the switch $S_2$ is turned OFF, and hence, the body-diode of $S_1$ begins to conduct due to the energy stored in the $L_f$. In this stage, the inductor current $i_{L_f}$ can be calculated by

$$i_{L_f}(t) = \frac{V_o}{2L_f}(t-t_0) + i_{L_f}(t_0)$$

(7)

Stage 2 [$[t_1, t_2]$: At $t_1$, $S_1$ is turned ON with ZVS. This stage ends when the switch $S_1$ is turned OFF at $t_2$.

Stage 3 [$[t_2, t_3]$: At $t_2$, $S_1$ is turned OFF, and then, the body-diode of $S_1$ begins to conduct due to the energy stored in the $L_f$. In this stage, the inductor current $i_{L_f}$ can be calculated by

$$i_{L_f}(t) = \frac{V_o}{L_f}(t-t_2) + i_{L_f}(t_2)$$

(8)

Stage 4 [$[t_3, t_4]$: At $t_3$, the switch $S_4$ is turned ON with ZVS. This stage ends when $i_{L_f}$ returns to zero, and the diodes $D_s$ and $D_f$ are OFF naturally with zero current and without reverse-recovery loss.

Stage 5 [$[t_4, t_5]$: At $t_4$, $i_{L_f}$ returns to zero. The diode $D_3$ is ON, which results in a zero voltage-level of $V_o$. Therefore, the inductor $L_f$ is charged by the input source, and the current $i_{L_f}$ can be calculated as,

$$i_{L_f}(t) = \frac{V_o}{L_f}(t-t_4)$$

(9)

Stage 6 [$[t_5, t_6]$: At $t_5$, the switch $S_3$ turns OFF. Since the current $i_{L_f}$ is positive, the diode $D_4$ begins to conduct. Hence, the input source and the energy stored in the inductor $L_f$ are delivered to the load. In this stage, the capacitor $C_{o1}$ is charged, while $C_{o2}$ is discharged. The inductor current $i_{L_f}$ is calculated as,

$$i_{L_f}(t) = \frac{V_o}{L_f}(t-t_5) + i_{L_f}(t_5)$$

(10)

Since the voltage of the flying capacitor $C_o$ is equal to the voltage of the $C_{o1}$, the drain-source voltage of the switch $S_6$ is clamped to zero.

Stage 7 [$[t_6, t_7]$: At $t_6$, the switch $S_6$ turns ON with zero-voltage and zero-current. The power is transferred to the load from the source continuously in this stage. Similar operation is conducted in the rest stages of the switching period.

2) Buck-DCM Mode

If the equivalent secondary duty cycle, $D_S$, decreases to zero, the converter operates at the boundary between Buck-CCM mode and Buck-DCM mode. In this scenario, if the output power or the normalized voltage gain decreases

$$D_p \equiv \frac{V_o}{2NV_{in}} \equiv G$$

(6)
the Buck-DCM mode. Suppose that the switches $S_5$ and $S_6$ are always in the OFF state. There are five switching stages in half of the switching cycle, and the corresponding equivalent circuits are shown in Fig. 12.

Stage 1[$t_s$, $t_1$] and Stage 2[$t_1$, $t_2$]: The operating principles of the Stage 1 and Stage 2 in the Buck-DCM mode are similar as that of the Stage 1 and Stage 2, respectively, in the Buck-CCM mode. In these two stages, the switch $S_1$ is turned ON with ZVS at $t_s$, the energy stored in the inductor $L_f$ is transferred to the load, and finally the inductor current $i_{lf}$ decreases to zero at $t_2$.

Stage 3[$t_2$, $t_3$] [Fig. 12(a)]: At $t_2$, $i_{lf}$ decreases to zero, and the diodes $D_3$ and $D_4$ are OFF with ZCS. Since $i_{lf}=0$, all the rectifying diodes are kept in the OFF state in this stage. There is no power transferred between the input and output.

Stage 4[$t_3$, $t_4$] [Fig. 12(b)]: At $t_3$, the switch $S_3$ is turned OFF with zero-current.

Stage 5[$t_4$, $t_5$] [Fig. 12(c)]: At $t_4$, the switch $S_5$ is turned ON with zero-current. The diodes $D_1$ and $D_2$ begin to conduct due to the positive voltage of $v_p$. Hence, the input source transfers power to the load, and the inductor current $i_{lf}$ increases linearly,

$$i_{lf}(t) = \frac{Nv_m - \frac{v_p}{2}}{L_f} (t - t_4) \quad (11)$$

This stage ends when the switch $S_1$ is turned OFF at $t_5$, and the second half of the switching cycle begins.

IV. PERFORMANCE ANALYSIS AND DISCUSSION

A. Output Power and Voltage Gain Analysis

1) Boost Mode

According to the operational principle of the Boost-CCM mode and waveforms shown in Fig. 5, we have: $i_A(t_0)=i_A(t_s)$, and $i_A(t_5)=0$. Then, based on (1)~(5), the values of $i_A(t_0)$, $i_A(t_s)$, and $\Delta T_2$ can be derived as,

$$i_{lf}(t_s) = \frac{V_o}{4f_sL_f} (1 + G)(G - D_sG - 1) \quad (12)$$

$$i_{lf}(t_5) = \frac{V_o}{4f_sL_f} 2D_sG - 1 \quad (12)$$

$$\Delta T_2 = t_5 - t_s = \frac{1}{2f_s} (1 - G(1 - D_s)) \quad (12)$$

where $f_s$ is the switching frequency. Then, the average output power $P_o$ can be calculated,

$$P_o = \frac{V_o^2}{16f_sL_f} (G + 1)(1 + 4D_s - 4D_s^2) - G^2 (2 - 4D_s + 2D_s^2) \quad (13)$$

On the other hand, based on (12) and $i_A(t_0)=0$, the boundary condition of Boost-CCM mode can be derived as,

$$D_{sb} = 1 - \frac{1}{G} \quad (14)$$

which means that the converter operates in the Boost-CCM mode if $D_s \geq D_{sb}$, and in the Boost-DCM mode if $D_s < D_{sb}$.

The same analysis can be performed for the Boost-DCM mode. When the converter operates in the Boost-DCM mode,
the current value \( i_L \) at \( t_2 \) can be given as follows,
\[
i_L(t_2) = \frac{V_o}{4f_L L_S} \frac{D}{G}
\]
(15)

and the output power is,
\[
P_{o, \text{Boost–DCM}} = \frac{V_o^2}{16f_L L_S} \frac{D_S^2}{G(G-1)}
\]
(16)

According to (13) and (16), the curves of the output power, which is normalized by power base \( P_o=(V_o^2)/(16f_L L_S) \), versus the secondary-side equivalent duty-cycle \( D_S \) can be obtained. The curves of the voltage gain \( G \) is shown in Fig. 13(b), where \( Q \) is the characteristic factor and defined as follows,
\[
Q = \frac{16L_f f_S}{R_o}
\]
(18)

2) Buck Mode

According to the operational principles of the converter in the Buck-CCM, the waveforms shown in Fig. 9, and (6)–(10), the current values \( i_L(t_1), i_L(t_2), i_L(t_3) \), and the time interval \( \Delta T_S \) can be derived as follows,
\[
\begin{align*}
i_L(t_1) &= \frac{V_o}{4f_L L_S} \frac{-D_S(G+1)+G^2+G-2}{G+2} \\
i_L(t_2) &= \frac{V_o}{4f_L L_S} \frac{-D_S(G+1)}{G+2} \\
i_L(t_3) &= \frac{V_o}{4f_L L_S} \frac{2D_S}{G(G+2)} \\
\Delta T_S &= t_4 - t_3 = \frac{1}{2f_S} \frac{GD_S+2-G-G^2}{G+2}
\end{align*}
\]
(19)

Then the output power can be calculated and given as (20).

On the other hand, according to the waveforms shown in Fig. 9, the condition that allows the converter work in the Buck-CCM mode is \( i_L(t_2)<0 \), which yields \( D_S>0 \). It means, if the primary-side duty-cycle \( D_o=G \), the converter will work in the Buck-CCM mode if and only if \( D_S>0 \).

As illustrated in Fig. 11, the operation of the Buck-DCM mode is very simple, and the output power can be given as follows,
\[
P_{o, \text{Buck–DCM}} = \frac{V_o^2}{16f_L L_S} \frac{D_S^2(1-G)}{G^2}, \quad 0 \leq D_o \leq G
\]
(21)

Substitute (17) and (18) into (20) and (21), the normalized voltage gain versus the equivalent duty cycle can be derived. Meanwhile, for a given \( Q \), the voltage gain \( G_B \) at the boundary of Buck-DCM and Buck-CCM modes can be derived as follows,
\[
G_B = 1 - Q
\]
(22)

The curves of the output power with different voltage gains,
TABLE I ZVS CONDITIONS OF PRIMARY SIDE SWITCHES

<table>
<thead>
<tr>
<th>Mode</th>
<th>$S_1$&amp;$S_2$ Conditions</th>
<th>$S_3$&amp;$S_4$ Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boost-CCM</td>
<td>$i_{L_f}(t_0) \leq -i_{L_f,zd,\min}$</td>
<td>N/A</td>
</tr>
<tr>
<td>Boost-DCM</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Buck-CCM</td>
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</tr>
<tr>
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<td>N/A</td>
</tr>
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</table>

TABLE II ZVS CONDITIONS OF BUCK MODE

<table>
<thead>
<tr>
<th>Mode</th>
<th>$S_1$&amp;$S_2$ Conditions</th>
<th>$S_3$&amp;$S_4$ Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck-CCM</td>
<td>$D_3 \geq \frac{4f_sL_fC_{oss}}{(G+1)N^2T_d}$</td>
<td>$D_3 \geq \frac{(G+2)f_sL_fC_{oss}}{(G+1)N^2T_d}$</td>
</tr>
<tr>
<td>Buck-DCM</td>
<td>$D_4 \geq \frac{1}{(1-G)} \frac{4f_sL_fC_{oss}}{N^2T_d}$</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Fig. 15.** Equivalent circuit during the dead time: (a) $S_1$ or $S_2$ is discharged, (b) $S_3$ or $S_4$ is discharged.

**Fig. 16.** Low frequency small-signal model of the proposed converter.

CCM operation range increases with a larger characteristics factor $Q$, which means the CCM operation range is proportional to the value of high-frequency-link inductor $L_f$ and output power. For a given duty cycle and output voltage, the output power decreases as the voltage gain increases. Therefore, the maximum voltage gain and the maximum output power must be taken into account for the parameter design, i.e. the value of the inductor $L_f$ and the switching frequency, of the converter. From the point of view of output ripples, the characteristic of the proposed AC-TLR is very similar to a conventional Boost converter. For a given output current, DCM operation will lead to higher current ripples and voltage ripples on the output side due to high peak value of $i_{L_f}$. Therefore, CCM operation is better for heavy load output, while DCM operation only occurs in light load conditions.

### B. Soft-Switching Performance

According to the operating principles of different modes, it has been shown that ZCS soft-switching of all the rectifying diodes in the AC-TLR are achieved within the whole operation range. For the active switches, $S_3$ and $S_4$, in the AC-TLR, the operating principles and waveforms (in Fig. 5, Fig. 7, Fig. 9 and Fig. 11) show that the drain-source voltage of $S_3$ will decrease to zero if and only if the current $i_{L_f}$ flows through $D_1$ and $D_2$, while the drain-source voltage of $S_4$ will decrease to zero if and only if $i_{L_f}$ flows through $D_3$ and $D_4$. It means ZVS soft-switching of $S_3$ and $S_4$ can be achieved if and only if the converter supplies power to the load. Therefore, ZVS of the active switches, $S_3$ and $S_4$, in the AC-TLR is independent of the operating conditions of the converter and the output capacitance of $S_1$ and $S_2$, and it can be achieved within the whole operation range.

If the output capacitances of the primary-side MOSFETs are taken into account, the ZVS of the primary-side switches will be affected by the values of output capacitance, dead time, and high-frequency-link inductors when switches are turned ON/OFF. For simplicity, the output capacitances of the primary-side switches are assumed to be linear and equal to $C_{oss}$. If $C_{oss}$ can be discharged to be zero during the dead time, $T_{di}$, by the high-frequency-link inductor current $i_{L_f}$, the ZVS of corresponding MOSFET can be realized. Because the value of high-frequency-link inductor $L_f$ is much higher (more than one thousand times) than $C_{oss}$, $i_{L_f}$ can be seen as constant and $L_f$ can be seen as a current source during the dead time. Assuming the value of $i_{L_f}$ during the dead time is $I_{L_f,zd}$, the equivalent circuits of the primary-side upper switches, $S_1$ or $S_2$, and lower switch, $S_3$ or $S_4$, are discharged by $L_f$ during the dead time are shown in Fig. 15.

As shown in Fig. 15, the following condition must be satisfied to discharge $C_{oss}$ to zero during the dead time

$$I_{L_f,zd} \geq \frac{2V_{oss}}{NT_d} = I_{L_f,zd,\min}$$

(B23)

Basing on Fig. 15 and (B23), the ZVS conditions for the primary side switches in different operation modes are listed in Table I.

Substituting (12) and (B23) into the equations in Table I, the ZVS condition for the Boost-CCM mode can be obtained as,

$$D_3 \geq \frac{1}{G} \frac{4f_sL_fC_{oss}}{(G+1)N^2T_d}$$

(B24)
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By following the same analysis procedures, the ZVS conditions of Buck-CCM and Buck-DCM can be obtained as well and listed in Table II.

From (14), (24) and equations in Table II, it can be seen that ZVS of all of the primary-side switches can be always achieved in the Boost-CCM and Buck-CCM modes if \( C_{oss} \) is zero, and ZVS of \( S_1 \& S_2 \) can be always achieved as well in the Buck-DCM mode if \( C_{oss} \) is zero. But the ZVS range will be reduced if the \( C_{oss} \) is not zero. It should be noted that discussion on ZCS is of no sense for MOSFETs if ZVS is not achieved, because there must be switching loss due to the discharging of \( C_{oss} \) when the switch is gating ON.

C. Small-Signal Model

Because the topology and operation principles of the proposed converter are similar to the DAB and SDAB converters, a current source based model (as shown in Fig. 16) is developed for the proposed converter for small-signal analysis by modifying the current source model of the DAB converter, which is presented in [26][27]. The detailed modeling process has been presented in [18][27]. Since the modeling method is not the focus of this paper and limited by the page number, only the Boost-CCM is analyzed here to show the effective of the current-source-based model.

The output current \( I_o \) in steady state can be obtained from (1)-(5) for an arbitrary secondary-side duty-cycle \( D_s \) as,

\[
I_{o\text{-Boost--CCM}}(D_s) = \frac{2NV_{in}(G+1)(1+4D_s-4D_s^2) - G^2 (2-4D_s+2D_s^2)}{16f_L f_s} (G+2) (25)
\]

The control-to-output transfer function can be derived by keeping the input voltage \( V_{in} \) and applying a small disturbance \( \Delta D_s \) to the \( D_s \), which causes a small disturbance \( \Delta I_o \), and produces a disturbance \( \Delta V_{o} \) around \( V_{o} \). Then the small-signal model for a resistive load shown in Fig. 16 can be obtained as,

\[
G_{d\text{-Boost--CCM}}(s) = \frac{\Delta V_{o}(s)}{\Delta D_s(s)} = \frac{NV_{in}(G+1)(1-2D_s)+G^2(1-D_s)}{2f_L f_s (G+2)^2} R_s \frac{1}{1+sR_C} \]

where.

Fig. 17 shows the comparison of the analytical result of (26) with the simulation result by using PSIM. The comparison is carried out under the following conditions: \( V_{in}=48V, V_{o}=380V, P_o=500W, f_s=100kHz, L_f=41.8uH, C_{oss}=330uF, N=23/6, D_s=0.228 \). It can be seen that the analytical result agrees with the simulation result very well, which verifies the effective of the current-source-based model. Based on this model, the controller has been designed.

D. Design Considerations

The soft-switching performance is achieved by using the phase-shift modulation. To achieve high conversion efficiency, the focus should be on the conduction losses. As analyzed above, the performance of the AC-TLR-based FB-IBB converter is mainly affected by the characteristic factor \( Q \). A 500W prototype operating at 100kHz with 40V-56V input voltage and 380V output voltage for battery discharging is implemented to test the main design considerations of \( Q \).

The root-mean-square (RMS) currents of the high frequency inductor \( L_f \) normalized with load current are calculated by using MathCAD to indicate the conduction losses, which are shown in Fig. 18. It can be seen that when \( G \) is close to 1.0, a smaller \( Q \) value means less conduction losses and is beneficial for efficiency enhancement. However, smaller \( Q \) will lead to high conduction loss if \( G \) is far away from 1.0. If \( G<1 \), a larger \( Q \) value results in a higher efficiency. However, if \( G>1 \), \( Q=0.3 \) will make the conduction loss get worse in the range of \( G>0.9 \). Taking these factors into consideration and to achieve high conversion efficiency within a wide operation range, \( Q=0.2 \) is a recommended choice. For the design example with \( f_s=100kHz, P_o=500W \) and \( V_{o}=380V, Q=0.2 \) means the value of \( L_f \) is about 40uH.

Once \( Q \) is determined, the turns ratio of transformer can be selected according to the range of \( G \) and the maximum efficiency point. In this design, the maximum efficiency point is located at the 52V input voltage where the minimum conduction loss is achieved with normalized voltage gain \( G=0.95 \) and \( Q=0.2 \), as shown in Fig. 18. Substituting \( G=0.95, V_{in}=52 \) and \( V_{o}=380 \) into (1), the turns ratio \( N \) is 3.84.

V. EXPERIMENTAL VERIFICATION AND ANALYSIS

A 500W prototype of the proposed FB-IBB converter
shown in Fig. 4 is built to verify the feasibility and effectiveness of the proposed AC-TLR and its derived IBB converters. The specifications of this prototype are listed in Table III. The operation range and soft-switching range of the primary-side switches are calculated and shown in Fig. 19 based on the parameters listed in Table III. The dead time is set at 100ns. It can be seen that the operation ranges of Boost-DCM and Buck-DCM modes increase when the normalized voltage gain far away from 1.0. The ZVS of the \( S_1 \) and \( S_2 \) is easier to realize than \( S_3 \) and \( S_4 \). Therefore, the ZVS region of \( S_1 \) and \( S_2 \) is wider than \( S_3 \) and \( S_4 \). Meanwhile, it can be seen that CCM operation is better than DCM operation for the soft-switching of primary-side switches.

Fig. 20 shows the experimental waveforms of the converter in the Boost-CCM mode, which are tested under 40V input voltage with normalized voltage gain \( G>1 \). Three voltage-levels can be seen from the voltage waveform of \( v_S \) in Fig. 20(a). The switching waveform of \( i_Lf \) in Fig. 20(a) coincides with the theoretical waveform in Fig. 5 pretty well, which verifies the effectiveness of the analysis. Meanwhile, ZVS of the primary side switches \( S_1 \) and \( S_2 \) has been achieved as shown in Fig. 20(b). Since all the primary-side switches work in the same pattern symmetrically, ZVS is accomplished for all of them. Moreover, ZVS is also achieved for the secondary-side switches \( S_3 \) and \( S_4 \) as shown in Fig. 20(c).

The experimental waveforms in the Boost-DCM mode with 90W output power are shown in Fig. 21. Three voltage-levels, including the zero voltage-level, can be seen from the waveform of \( v_S \) in Fig. 21(a). From Fig. 21(b) and (c), it can be seen that ZVS/ZCS turn OFF is achieved for the primary-side switches, but ZVS turn ON is lost due to the lack of energy to discharge output capacitances of MOSFETs. Meanwhile, ZVS can also be achieved for the secondary-side switches \( S_3 \) and \( S_4 \) as shown in Fig. 21(d). It should be noted that, when the converter works in the Boost-DCM mode and the inductor current \( i_Lf \) reaches zero, the oscillation of the \( v_S \) is caused by the resonance between the inductor \( L_f \) and the parasitic capacitances of these switches.

Fig. 22 shows the experimental waveforms in the Buck-CCM mode. The primary-side and secondary side voltages \( v_P, v_S \) and the driving voltages of the switches \( S_1, S_4 \) and \( S_3 \) are shown in Fig. 22(a) and (b). It can be seen that both the primary-side full-bridge inverter and the secondary-side AC-TLR generate three voltage levels due to the dual phase-shift control in the Buck-CCM mode. The waveforms coincide with the analysis of Fig. 9 pretty well. Meanwhile, ZVS have been achieved for all the primary-side
switches and the secondary-side switches, as shown in Fig. 22(c) and (d).

The experimental waveforms in the Buck-CCM mode with \( G < 1 \), (a) voltage produced by the primary-side full-bridge inverter \((v_P)\), voltage produced by the AC-TLR \((v_S)\), and current through the inductor \((i_{L_f})\), (b) driving voltages of \( S_1 \) \((v_{GS1})\), \( S_4 \) \((v_{GS4})\), \( S_5 \) \((v_{GS5})\), and \( i_{L_f} \), (c) driving voltages \((v_{GS1}, v_{GS4})\) and drain-source voltages \((v_{DS1}, v_{DS4})\) of \( S_1 \) and \( S_4 \), (d) driving voltages \((v_{GS5}, v_{GS6})\) and drain-source voltages \((v_{DS5}, v_{DS6})\) of \( S_5 \) and \( S_6 \).

The experimental waveforms in the Buck-DCM mode with \( G > 1 \), (a) voltage produced by the primary-side full-bridge inverter \((v_P)\), voltage produced by the AC-TLR \((v_S)\), and current through the inductor \((i_{L_f})\), (b) driving voltages \((v_{GS1})\), \( v_{GS4} \), \( v_{GS5} \) and \( i_{L_f} \), (c) driving voltages \((v_{GS1}, v_{GS4})\) and drain-source voltages \((v_{DS1}, v_{DS4})\) of \( S_1 \) and \( S_4 \), (d) driving voltages \((v_{GS5}, v_{GS6})\) and drain-source voltages \((v_{DS5}, v_{DS6})\) of \( S_5 \) and \( S_6 \).

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Achieved for the switch \( S_1 \), but ZVS cannot be achieved for \( S_5 \).

The efficiency curves versus output power under different input voltages are shown in Fig. 24. When the input voltage is 40V, the maximum efficiency is 96.6% and the efficiency at full-load is 95.6%; when the input voltage is 50V, the maximum efficiency is 97.3% and the efficiency at full-load is 96.7%; when the input voltage is 56V, the maximum efficiency is 96.8% and efficiency at full-load is 96.6%. To evaluate the performance of the proposed topology, the
isolated-boost topology presented in [23] is selected as the reference for some quantitative comparisons. In the topology in [23], a full-bridge circuit and four rectifying diodes are used, and the voltage stress of rectifying diodes is half of the input voltage as well. The input and output voltages of experimental prototype in [23] are the same as the proposed converter. The experimental results in [23] indicate that the conversion efficiency of the isolated boost converter decreases as the input voltage decreases. As a result, trade-offs among the efficiencies under maximum, normal and minimum input voltages are very difficult to make. The highest efficiency of the isolated boost converter occurs when the input voltage is 56V. When the input voltage is 56V, the maximum efficiency of the isolated-boost converter is only 96.3% and the efficiency at full-load is only 95.6%, which are lower than the proposed topology. It is because the voltage stress on the primary-side switches in the isolated-boost converter is much higher than the input voltage. 200V-rated MOSFETs have to be used for a 40V-56V input voltage application. In comparison, 80V-rated MOSFETs can be employed in the proposed converter.

VI. CONCLUSION
An active-clamped three-level rectifier (AC-TLR), which roots in the diode-clamped three-level inverter, is proposed to fulfill the requirements of high output voltage and isolated Buck-Boost conversion. The voltage stress on the components in the AC-TLR is reduced to half of the output voltage, which enhances the voltage transfer ratio. Meanwhile, low voltage rated devices with lower conduction and switching losses are used to improve efficiency. Isolated Buck-Boost (IBB) converters based on the proposed AC-TLR are developed. A full-bridge IBB converter is taken as an example for the detailed analysis of the proposed AC-TLR. An optimized phase-shift control strategy is proposed for the full-bridge IBB converter. The operating principles, output characteristics, and soft switching performances are discussed. The theoretical analysis and experimental results indicate that soft-switching within wide operation range has been achieved in the proposed converter. Hence, high efficiency has been achieved within a wide operation range. As a novel solution for IBB converters, the proposed AC-TLR and its derived IBB converter is an good candidate for high efficiency isolated Buck-Boost conversion systems with high output voltage.

VII. REFERENCES


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