A Bidirectional Modular Multilevel DC–DC Converter of Triangular Structure

Kia Filsoof, *Student Member, IEEE*, and Peter W. Lehn, *Senior Member, IEEE*

***Abstract*—In this paper, a novel bidirectional modular multilevel dc–dc converter is proposed. The proposed topology, named the triangular modular multilevel dc–dc converter (TMMC), can achieve equal power sharing among its modules over a broad range of conversion ratios. The proposed control algorithm provides localized control of modules which enhances the converter's dynamic performance and design flexibility. A 1.7-kW experimental implementation of the converter is shown to achieve an efficiency of 95.9% and 96.2% in step-up and step-down modes, respectively. Significant reductions in the input current and output voltage ripples are observed through the interleaved operation of the converter. The TMMC also provides multiple fixed voltage nodes which makes it suitable as a multiple-input multiple-output converter.**

***Index Terms*—DC–DC power conversion, high-power converters, modular multilevel converters (MMCs), multiple-input multiple-output converters.**

I. Introduction

RECENTLY, modular multilevel converters (MMCs) have captured the attention of the high-power [9] and medium-power [1] communities. Fully modular converters benefit from several advantages such as: 1) the ability to control the voltage and current stresses applied to their components through incorporation of identical modules in series or parallel; 2) enhanced reliability through installation of redundant modules; 3) reduced design, manufacturing, installation, and maintenance costs due to standardization of the overall product cycle; and 4) higher power density due to minimized input and output current ripples through interleaving schemes. In this paper, a modular multilevel dc–dc converter topology is developed. Though targeted for medium-voltage applications, examination of the topology's capabilities shows that it may be employed as a multiple-input and/or multiple-output converter, thus making variants of the converter suitable for low-power applications as well.

Several effective modular multilevel dc–dc converters have been proposed in the literature. In [1], a modular multilevel capacitor-clamped dc-dc converter is proposed. The magnetic-less structure of this topology makes it well suited for automotive applications [2], [3]. The topology also has a bidirectional structure and may support multiple sources or loads [4]. However, due to the switched-capacitor nature of this topology, a deliberate startup procedure [5] is required to avoid current spikes. The capacitor-clamped topology is further investigated and modified for soft-switching [6], [7] and optimal design [8]. A few disadvantages associated with the topology of [1] are: 1) it is restricted to integer-only conversion ratios and 2) its modules' capacitors are exposed to different steady-state voltage stresses, making the topology non-modular from a manufacturing and design perspective.

Modular multilevel dc–dc converters based on the dc–ac MMC topology of [9] are derived in [10]–[12]. The inherent operating mechanism common among these topologies is to circulate ac currents in order to achieve energy balance between their modules. While such operation permits the development of dc–dc converters for very high voltage levels, circulating ac currents lead to increased conduction losses that may be avoided by the proposed converter in medium-voltage applications.

Modular converters based on isolated dc–dc topologies are proposed in [13] and further investigated and modified in [14]–[17]. In applications where isolation is not a requirement, the weight, parasitics, losses, and cost associated with transformers add to the system complexity and limit the expandability and operating power of such topologies. In addition, the expandability of these converters is limited due to transformer isolation rating requirements.

A modular multilevel dc–dc converter is proposed in [18] for interfacing supercapacitors to a dc bus in regenerative braking applications. The topology is constructed from a series connection of half-bridge converters with an output inductor.

In [19], a family of nonisolated modular resonant dc–dc converter topologies are proposed for high-power applications. These topologies enable static voltage sharing among identical modules which may be connected in series. Soft-switching is also realized with these converters. A variation to the step-up topology of [19] is proposed in [20]. Disadvantages with these topologies are the large size of the passive components, the high peak currents, and the challenges associated with dynamic voltage sharing during switch transitions.

The proposed topology, named the triangular modular multilevel dc–dc converter (TMMC) has a transformerless structure and does not suffer from high peak currents. Additionally, the proposed topology provides: 1) a fully modular structure by enabling equal module power sharing at a broad range of conversion ratios; 2) a bidirectional structure, making it suitable for a wide array of applications; and 3) localized control of its modules, enhancing its dynamic performance. Moreover, the

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The authors are with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, M5S 2J7 Canada (e-mail: kia.filsoof@mail.utoronto.ca; lehn@ecf.utoronto.ca).

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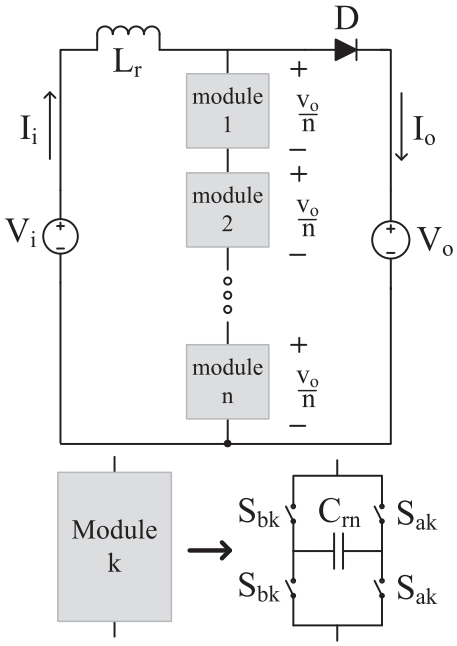


Fig. 1. Topology of [19] in step-up n-level configuration.

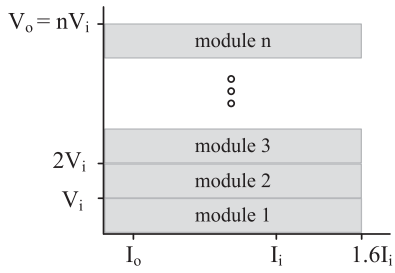


Fig. 2. Module power sharing illustration of the converter of Fig. 1 with $n = V_o/V_i$.

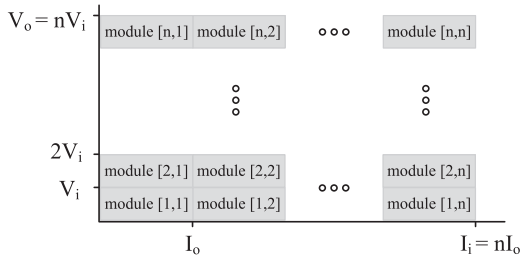


Fig. 3. Power sharing of a modular converter with better power sharing capability than that of Fig. 1.

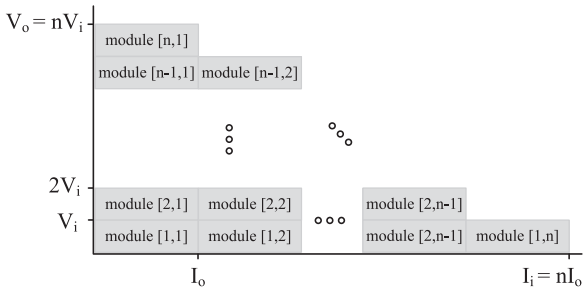


Fig. 4. Proposed power sharing diagram of an optimal modular dc–dc converter.

topology provides multiple fixed voltage nodes which may be utilized as either inputs or outputs. This qualifies the topology as a multiple-input multiple-output converter and makes it suitable as a scalable unified solution for a variety of power system architectures.

II. Derivation of the Proposed Topology

The proposed topology is derived based on an evaluation of the power sharing capability of the topologies of [19]. The evaluation measures the efficacy of a modular converter to share the voltage and current among its modules for a given power rating. This analysis is similar to investigating the switch utilization of a converter.

Consider topology of [19] configured as an n-level step-up converter as shown in Fig. 1. This converter employs n modules connected in series to support a high output voltage, with each module supporting a voltage of V_o/n. As mentioned earlier, this topology suffers from high peak input current due to resonance. This high peak input current, which is approximately 1.6 (π/2) times the average input current must flow through all the series modules. For simplicity, n is selected such that each module must withstand V_i. The resulting module power sharing of this converter for a given power rating is illustrated in Fig. 2. Each module carries $1.6I_i$ and is rated for a voltage of V_o/n. From this figure, it is implied that each module within this converter must therefore be rated at 1.6 I_iV_i V·A.

Based on the power sharing diagram of Fig. 2, a modular converter with better power sharing capability may be sought. An apparent improvement would be the utilization of hard-switched converters which experience peak inductor currents that are approximately equal to the average inductor current. In addition, a topology may be sought which would benefit from current sharing as well as voltage sharing through parallel connection of its modules. The module power sharing diagram of such a converter is shown in Fig. 3.

Unlike the converter of Fig. 1, each row of an optimally constructed converter need not process a current equal to the input current. For example, considering the top row in Fig. 3 where a net voltage of nV_i is realized, only one module might be needed to process the output current, I_o. Similarly, at lower rows, where a lower net voltage is realized, more parallel modules would be required to process the higher current. The power sharing diagram of such a topology is shown in Fig. 4. A modular dc–dc converter with such power sharing capability has a theoretically optimal module utilization and is considered as a frame of reference for derivation of the proposed topology.

As noted, a converter with a power sharing of Fig. 4 would have approximately half the number of modules as that of Fig. 3. This implies significant reduction in the required amount of silicon area.

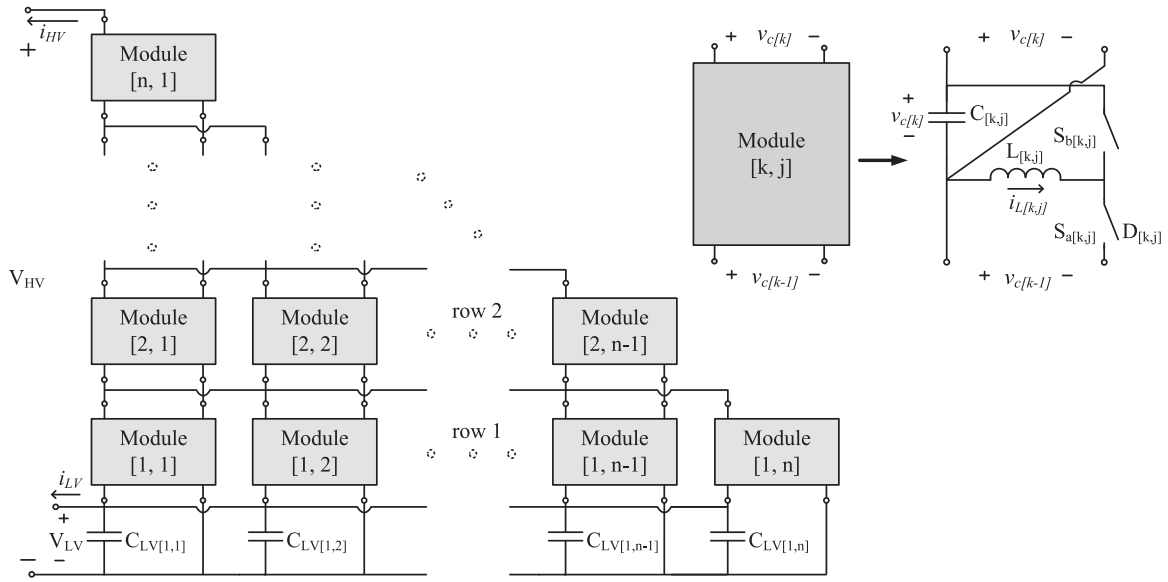


Fig. 5. Proposed bidirectional n-level TMMC and its corresponding single-module representation.

III. Proposed Converter Topology

The proposed TMMC topology [21] is configured as a general n-level structure as shown in Fig. 5. TMMC's modules are constructed from buck-boost converters as shown on the top right corner of Fig. 5. The TMMC is bidirectional such that the high-side voltage ($V_{\rm HV}$) and low-side voltage ($V_{\rm LV}$) may readily be used as either input or output. It is noted that the proposed topology's structure resembles that of the power sharing diagram of Fig. 4. While the power sharing capability of the TMMC is not identical to that of Fig. 4, it has a significantly reduced silicon area requirement as compared to the topology of [19] (lower than 50% for conversion ratios lower than five). Detailed discussion on this topic is outside the scope of this paper.

The single-column structure of the TMMC is similar to the battery charge equalizer circuit first proposed in [22] and later applied to PV applications [23] for equalizing series-stacked PV panel voltages [23]–[27]. This structure has also been recently employed for differential power processing of digital systems [28].

As noted from the TMMC's structure in Fig. 5, there are n modules in parallel on the first row to process the high current on the low-voltage side, and at higher rows where a higher net voltage is realized, fewer modules are connected in parallel. The low-voltage side's parallel capacitors ($C_{\rm LV[j,]}$) are required simply for filtering reasons and are not inherent to the proposed topology's structure.

Semiconductor switches such as MOSFETs or IGBTs may readily be utilized as the active switches. For the bidirectional operation, both switches would be of active type. For step-up only operation, switch S_a would be of active type and switch S_b could be a diode. Conversely, for step-down only operation, switch S_a could be a diode and switch S_b would be of active type. Switches S_a and S_b are operated in complementary of each other.

TABLE I
Number of Switch Requirements for the TMMC (Under Integer-Only Conversion Ratio)

Gain	# of rows	# of switches
2	1	2
3	2	6
.	.	.
n+1	n	n(n+1)

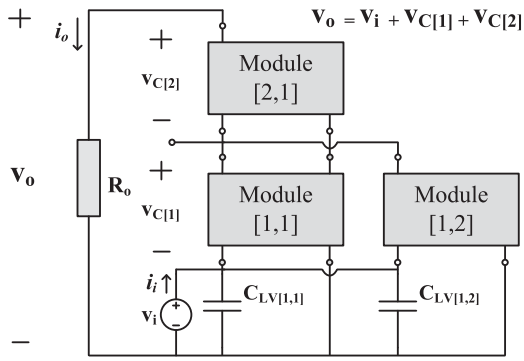


Fig. 6. Two-level configuration of the TMMC in the step-up mode.

In general, the TMMC modules are not restricted to the arrangement shown in Fig. 5, and alternative configurations exist. Furthermore, additional or fewer modules may be connected in parallel at any row, however, this paper will focus on this right-triangular structure which optimally utilizes the power sharing capacity of each module for single-input single-output applications. This will be further elaborated on the following sections.

The optimal conversion ratio to operate an n-level TMMC is $n+1$ as the converter may easily achieve equal voltage and current sharing among its modules under such configuration. An n-level TMMC may also be operated at other non-integer

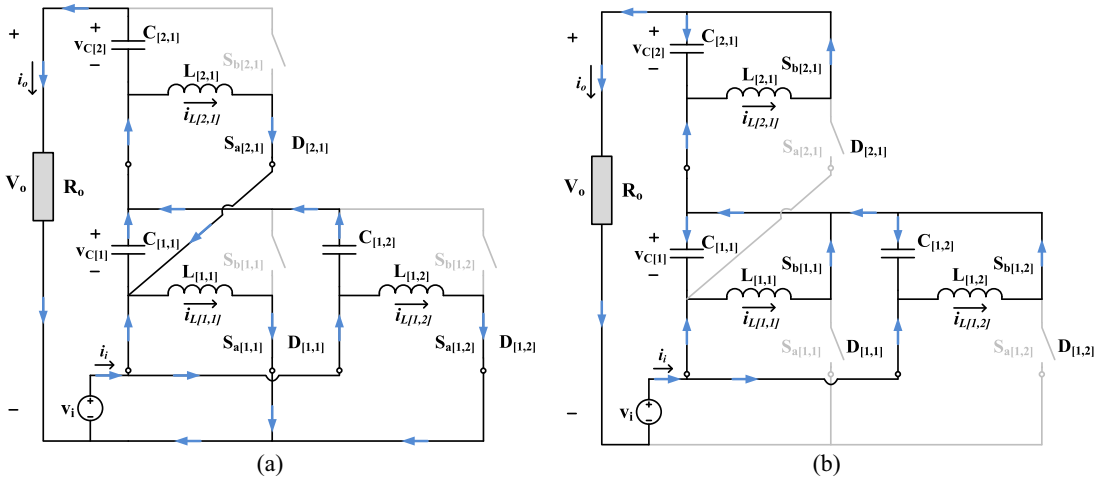


Fig. 7. Switching states of the two-level TMMC with corresponding current flow directions. (a) State 1: $S_{a[k,j]}$ ON, $S_{b[k,j]}$ OFF. (b) State 2: $S_{a[k,j]}$ OFF, $S_{b[k,j]}$ ON.

conversion ratios and still maintain equal module power sharing. An exception in this case would be the first row modules which would carry a current different than other row modules. Nevertheless, this may easily be compensated through addition or subtraction of modules in the first row. Assuming integer-only conversion ratios, the number of required rows and switches for a given conversion ratio are shown in Table I. Note that the number of required modules is half the number of required switches.

The remainder of this paper is focused toward discussing the steady-state and dynamic behavior of the TMMC. To aid with visualization and understanding, the two-level structure is selected as the topology under analysis. All discussion is appropriately scalable to the n-level configuration.

The two-level TMMC configured in step-up mode is shown in Fig. 6. As specified, the output voltage is simply equal to the summation of the input voltage with the first and second row capacitor voltages. For step-down operation, the load and the source would simply be interchanged.

Fig. 7 shows the switching states and corresponding current flow directions of the two-level step-up TMMC under noninterleaved operation. In state 1, switches $S_{a[k,j]}$ are ON, while switches $S_{b[k,j]}$ are OFF. In this state, the modules' inductors are energized, with the first row modules' inductors energized from the input voltage source and the second row module's inductor energized through the first row modules' capacitors. Conversely, in state 2, switches $S_{a[k,j]}$ are OFF, while switches $S_{b[k,j]}$ are ON. In this state, each module's inductor is transferring energy to the corresponding module's capacitor.

IV. Proposed Control Algorithm and the Analytical Model

In this section, a control algorithm is proposed for the TMMC which provides localized control of all converter modules to result in the enhanced dynamic performance and overall design flexibility of the system. It also supports the possibility of a modular control design approach. A simplified analytical model

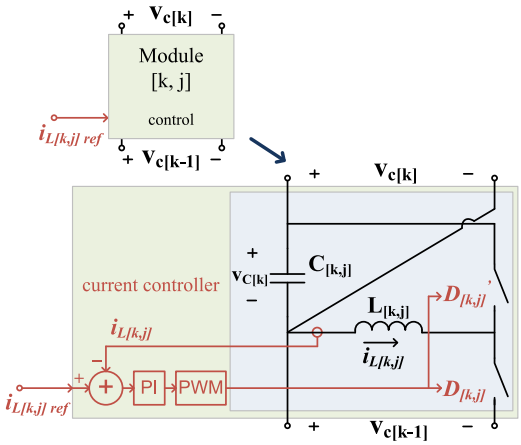


Fig. 8. TMMC single module representation with the internal current controller.

of the overall system is also provided based on the proposed control algorithm.

A. Proposed Control Algorithm

Each module within the TMMC is controlled through an internal current controller as represented in Fig. 8. The current reference for each module is provided through a voltage controller which effectively controls the capacitor voltages of the corresponding row.

The two-level TMMC in the step-up mode with its corresponding voltage and current controllers is shown in Fig. 9. A voltage controller on a given row controls the capacitor voltages of the particular row plus the capacitor voltages of the previous row. By controlling the summation of the neighboring rows' capacitor voltages, an interdependence is provided within the voltage controllers which enhances the dynamic behavior of the converter. The output of each voltage controller provides the reference current for all parallel modules on the particular row to result in equal current sharing. The reference for the voltage

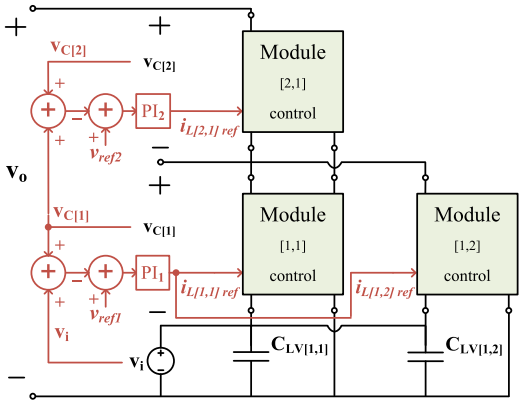


Fig. 9. Two-level TMMC in the step-up mode with corresponding control blocks.

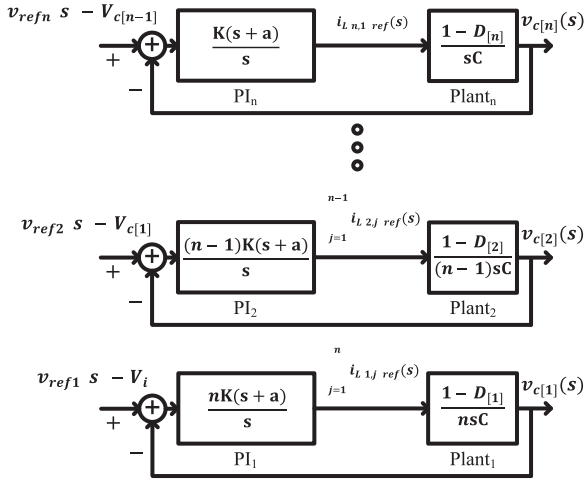


Fig. 10. Simplified analytical model of the closed-loop n-level TMMC.

controllers is set such that equal voltage sharing is achieved among all rows for a given input voltage and desired output voltage. It should be noted that unique voltage references may be provided to each row if desired; however, equal voltage and current sharing will be compromised.

To result in similar dynamic models between all rows, the PI control parameters are selected as follows:

1) The current controller parameters of all modules are the same and chosen such that the current controllers are at least ten times faster than the voltage controllers.
2) Since for a given row, k, of an n-level TMMC there exists $n-k+1$ parallel capacitors, the voltage controller gain parameter of that given row is multiplied by $n-k+1$ to result in similar dynamic behavior among other rows' capacitor voltages in case of a voltage reference step.

B. Analytical Model

A simplified analytical model of a closed-loop n-level TMMC is derived based on the proposed control algorithm. The following assumptions are applied to derive this analytical model:

1) Each module's inductor dynamic is ignored and treated as a current source since the inner loop current controllers are designed for a much faster response than the corresponding row's outer loop voltage controller.
2) The output current of each module is treated as a current sink with no dynamics. Any step in the load current is considered as a disturbance.
3) Interdynamics of neighboring rows' modules are ignored. Each row's capacitors' voltage is seen as a voltage source from the perspective of its neighboring row.
4) All modules are assumed identical, hence, the operating duty cycles of paralleled modules are assumed to be equal ($D_{[k,j]} = D_{[k]}$).

Through application of the aforementioned assumptions, each row of the TMMC may be modeled independently with combined dynamics of the parallel modules. Fig. 10 shows the derived analytical model of the n-level TMMC.

V. Steady-State Analysis

To aid with the design and further insight of the TMMC, a steady-state analysis of the proposed n-level topology in step-up mode is provided in this section. Equations are provided for obtaining the steady-state average and the peak-to-peak ripple current and voltage values. With slight modifications, these equations may also be applied to the step-down topology.

To simplify the analysis, the following assumptions are applied:

1) the small ripple approximation as discussed in [29];
2) $D_{[k,j]} = D_{[k]}$, $I_{L[k,j]} = I_{L[k]}$, $L_{[k,j]} = L$, $C_{[k,j]} = C$, $R_{L[k,j]} = R_L$, $R_{\mathrm{ON[k,j]}} = R_{\mathrm{ON}}$, where R_L and R_{ON} are the inductor's and transistor's internal resistances, respectively;
3) both switches, S_a and S_b, of modules are of active type;
4) the converter operates in a non-interleaved scheme;
5) for the sake of notational simplicity, we define $I_{L[n+1]} = I_o$, $V_{C[0]} = V_i$ and $D_{[n+1]} = 0$;

For an n-level step-up TMMC, the output voltage, inductor currents, and capacitor voltages may be obtained by the following equations:

$$V_o = \sum_{k=0}^{n} V_{C[k]}. \tag{1}$$

$$I_{L[k]} = \begin{cases} \dfrac{1}{(n-k+1)} \dfrac{\big((n-k)I_{L[k+1]} - (n-k-1)I_{L[k+2]}D_{[k+2]}\big)}{1-D_{[k]}}, \\ \qquad\qquad k \in \{1, 2, \ldots n-2\} \\ \dfrac{(n-k)}{(n-k+1)} \dfrac{I_{L[k+1]}}{1-D_{[k]}}, \qquad k = n-1 \\ \dfrac{I_o}{1-D_{[k]}}, \qquad k = n \end{cases} \tag{2}$$

$$V_{C[k]} = \frac{V_{C[k-1]}D_{[k]}}{1-D_{[k]}} - \frac{I_{L[k]}(R_L + R_{\mathrm{ON}})}{1-D_{[k]}}. \tag{3}$$

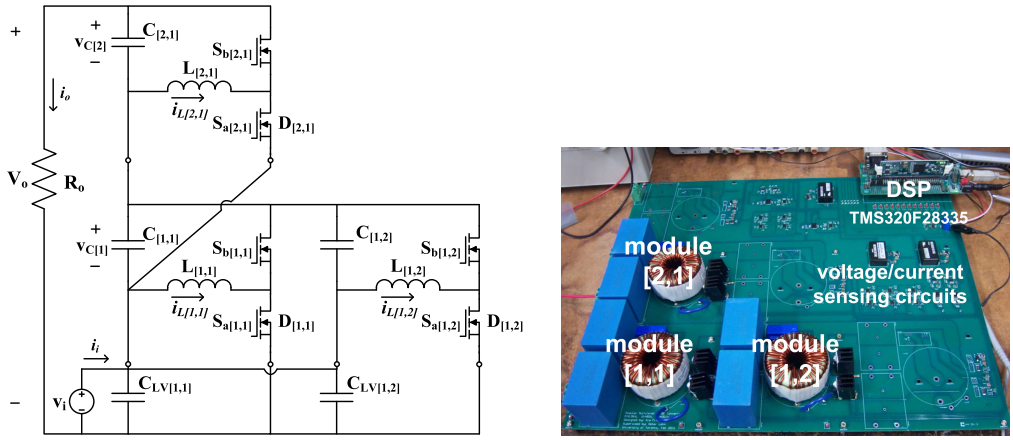


Fig. 11. Two-level TMMC. (a) TMMC experimental setup schematic in the step-up mode (the source and load are simply interchanged for the step-down operation). (b) TMMC experimental setup prototype.

The aforementioned set of equations may readily be solved as they result in $2n+1$ equations and $2n+1$ unknowns.

The peak-to-peak inductor current ripples may be obtained by the following equation:

$$\Delta I_{L[k]} = \frac{V_{C[k]} + I_{L[k]}(R_L + R_{\mathrm{ON}})}{L f_s}. \tag{4}$$

The peak-to-peak capacitor voltage ripple of a particular row is not as trivial to evaluate as it is affected by the operating point of its neighboring row. For a row k, if $D_{[k]} \geq D_{[k+1]}$, then

$$\Delta V_{C[k]} = \frac{((n-k+1)I_{L[k]} - I_o)(1-D_{[k]})}{(n-k+1)C f_s}. \tag{5}$$

If $D_{[k]} < D_{[k+1]}$ and $((n-k)I_{L[k+1]} + I_o - (n-k+1)I_{L[k]}) > 0$, then

$$\begin{aligned}\Delta V_{C[k]} = \frac{1}{(n-k+1)C f_s}\big(&((n-k)I_{L[k+1]} + I_o)D_{[k]} \\ &+((n-k)I_{L[k+1]} - (n-k+1)I_{L[k]} + I_o) \\ &\times (D_{[k+1]} - D_{[k]})\big).\end{aligned} \tag{6}$$

If $D_{[k]} < D_{[k+1]}$ and $((n-k)I_{L[k+1]} + I_o - (n-k+1)I_{L[k]}) \leq 0$, then

$$\Delta V_{C[k]} = \frac{((n-k)I_{L[k+1]} + I_o)D_{[k]}}{(n-k+1)C f_s}. \tag{7}$$

The peak-to-peak input current ripple equation is as follows:

$$\Delta I_i = n\left(I_{L[1]} + \frac{\Delta I_{L[1]}}{2}\right). \tag{8}$$

Due to the non-overlapping nature of the capacitor voltage waveforms, an exact expression for the output voltage ripple is cumbersome to obtain. However, an upper bound on the output voltage ripple may be expressed as follows:

$$\Delta V_o \leq \sum_{k=1}^{n} \Delta V_{C[k]}. \tag{9}$$

TABLE II
TWO-LEVEL TMMC SIMULATION AND EXPERIMENTAL SETUP PARAMETERS

Parameter	Value	Part Number
f_s	20 kHz	-
$L_{[k,j]}$	560 μH	CWS HF5712-561M-25AH
$C_{[k,j]}$, $C_{LV[1,j]}$	60 μF	EPCOS B32678G3606K
$S_{a[k,j]}$, $S_{b[k,j]}$	-	Infineon IPP200N25N3G

The active switches' static voltage and current ratings may be expressed as follows, respectively:

$$V_{\mathrm{Sa}[k,j]\mathrm{OFF}} \leq V_{C[k]} + V_{C[k-1]} + \frac{\Delta V_{C[k]}}{2} + \frac{\Delta V_{C[k-1]}}{2} \tag{10}$$

$$V_{\mathrm{Sb}[k,j]\mathrm{OFF}} \leq V_{C[k]} + V_{C[k-1]} + \frac{\Delta V_{C[k]}}{2} + \frac{\Delta V_{C[k-1]}}{2} \tag{11}$$

$$I_{\mathrm{Sa}[k,j]\mathrm{ON}} = I_{L[k]} + \frac{\Delta I_{L[k]}}{2} \tag{12}$$

$$I_{\mathrm{Sb}[k,j]\mathrm{ON}} = I_{L[k]} + \frac{\Delta I_{L[k]}}{2}. \tag{13}$$

In the special case of a lossless TMMC operating under the control algorithm proposed in Section IV-A, the operating conversion ratio may be approximated as follows:

$$\frac{V_o}{V_{\mathrm{in}}} = \frac{1 + D_{[1]}(n-1)}{1 - D_{[1]}}. \tag{14}$$

This resulting expression rises because in an ideal scenario, the proposed control algorithm would only vary the duty cycle of the first row modules and keep the duty cycle of all other row modules at 50% for the TMMC to operate at a given conversion ratio.

The equations provided in this section may be utilized to design a TMMC for a given converter specification.

VI. Simulation and Experimental Results

In this section, simulation and experimental results of a two-level TMMC are discussed. The schematic and prototype of the

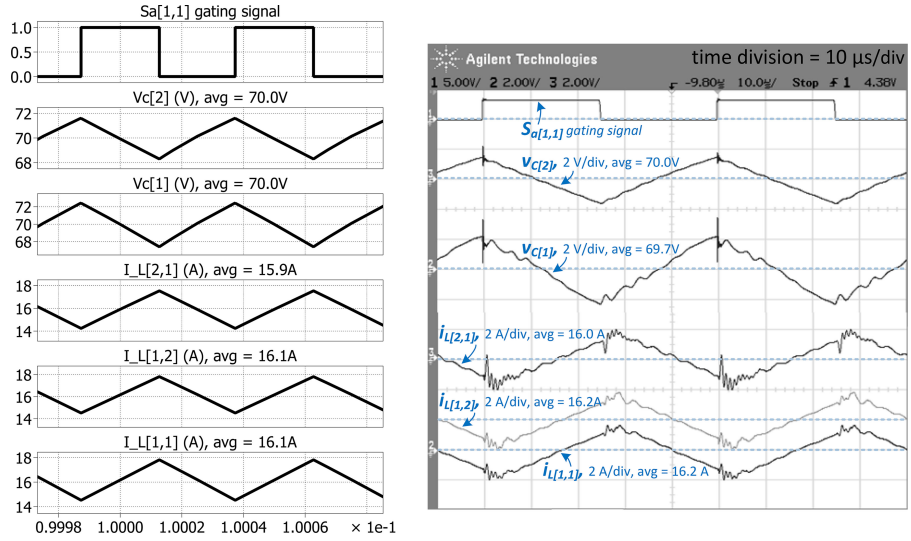


Fig. 12. Steady-state results of the two-level TMMC of Table II ($V_i = 70$ V, $P_i = 1.7$ kW, $V_o/V_i = 3$, $R_o = 26.9\,\Omega$). (a) Simulation results ($\eta = 96.5\%$). (b) Experimental results ($\eta = 95.9\%$). Voltage and current scope signals are ac coupled.

TABLE III
AVERAGE AND RIPPLE MEASUREMENTS OF THE NON-INTERLEAVED TWO-LEVEL TMMC ($V_i = 70$ V, $P_i = 1.7$ kW, $V_o/V_i = 3$, $R_o = 26.9\,\Omega$)

	Analytical	Simulated	Experimental
ΔV_o (V)	8.3	8.3	7.6
ΔI_i (A)	35.2	35.2	36.0
$V_{C[2]}$ (V)	70.0	70.0	70.0
$V_{C[1]}$ (V)	70.0	70.0	69.7
$I_{L[2]}$ (A)	15.8	15.9	16.0
$I_{L[1]}$ (A)	15.9	16.1	16.2
$\Delta V_{C[2]}$ (V)	3.3	3.3	3.3
$\Delta V_{C[1]}$ (V)	5.0	4.9	4.7
$\Delta I_{L[2]}$ (A)	3.3	3.2	4.0
$\Delta I_{L[1]}$ (A)	3.3	3.2	3.8

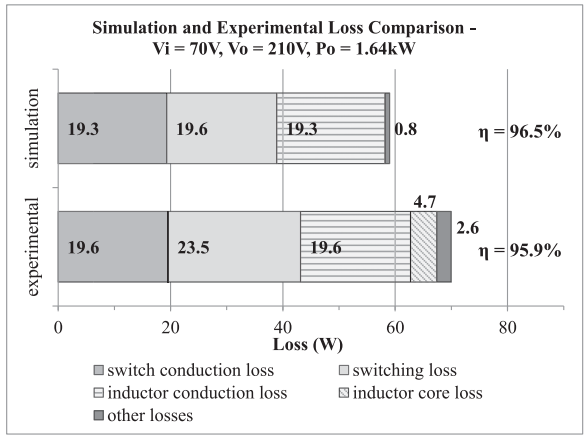


Fig. 13. Simulation and experimental loss comparison of the non-interleaved two-level step-up TMMC of Table II.

converter under test are shown in Fig. 11(a) and (b), respectively. The prototype PCB is laid out for a three-level TMMC, but only the two-level configuration is utilized in this paper.The circuit parameters are provided in Table II.

A. Steady-State Operation

The two-level TMMC of Table II is evaluated via simulation and experiment at an input power of 1.7 kW in the step-up mode. The converter is operated with an input voltage of 70 V at a conversion ratio of three ($V_o = 210$ V). Steady-state waveforms are shown in Fig. 12. It is noted that both simulation and experimental results are similar. As expected, equal voltage and current sharing is achieved between the capacitor voltages and inductor currents, respectively. The first row's inductor currents are marginally higher than the second row's due to losses. The average and ripple voltage and current measurements of the two-level TMMC under steady-state operation are tabulated in Table III. The experimental results match closely with the analytical and simulated results. Equations (1)−(9) were applied to compute the analytical values.

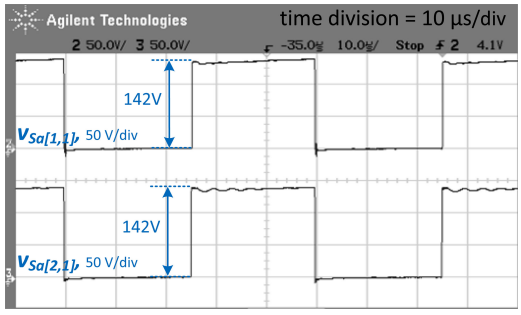
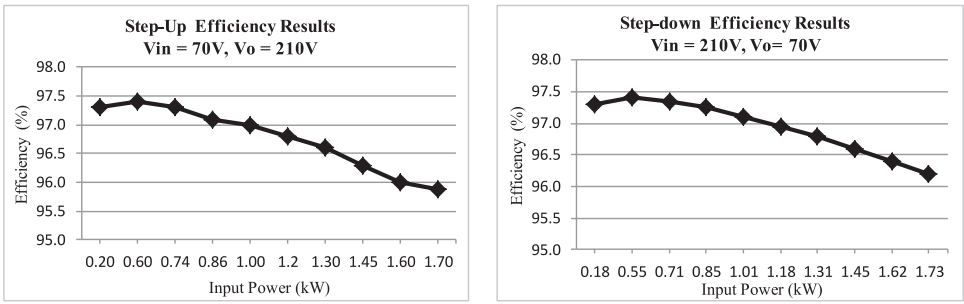


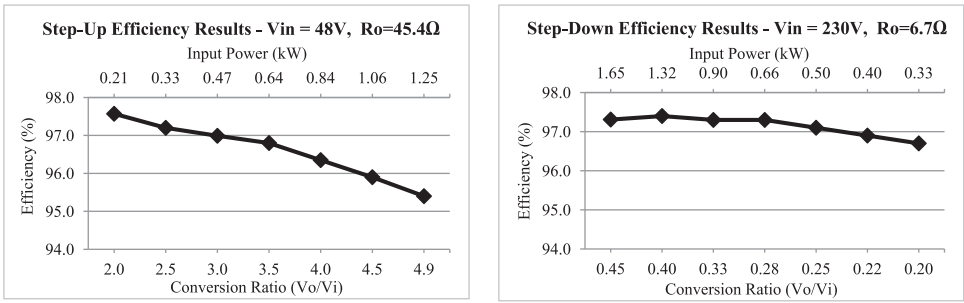
Fig. 14. Experimentally measured switch voltage waveforms of the two-level TMMC ($V_i = 70$ V, $P_i = 1.7$ kW, $V_o/V_i = 3$, $R_o = 26.9\ \Omega$).

The simulation model's efficiency is measured to be 96.5% which is 0.6% superior to the experimental system's (95.9%). This difference results from the omission of the magnetic core losses of inductive components and the PCB conduction loss



(a) (b)

Fig. 15. Experimental efficiency characteristic of the noninterleaved two-level TMMC with load variation in the (a) step-up and (b) step-down mode.



(a) (b)

Fig. 16. Experimental efficiency characteristic of the noninterleaved two-level TMMC with conversion ratio variation in the (a) step-up and (b) step-down mode.

in the simulation model. Fig. 13 depicts the comparison between the simulation model's and experimental setup's loss breakdowns. For the PLECS simulation model, the methods described in [30] and [31] were employed to model the conduction and switching losses.

Experimentally measured voltage waveforms of switches $S_{a[1,1]}$ and $S_{a[2,1]}$ are plotted in Fig. 14. As noted, both switches block a voltage of 142 V in the off state which is in accordance to the expected values as obtained by (10).

B. Efficiency Analysis

The power conversion efficiency of the two-level TMMC has been experimentally investigated under both step-up and step-down operation using the Yokogawa WT3000 high-precision power analyzer. The efficiency of the converter has been measured at operating power levels ranging from 200 W to 1.7 kW.

The efficiency characteristics of the converter with variation in the output load are plotted in Fig. 15. Similar results are observed in the efficiency characteristic of the step-up and step-down configurations with measured efficiencies of 95.9% and 96.2% at the rated power of 1.7 kW, respectively. The efficiency characteristics of the converter with variation in the conversion ratio are also obtained and plotted in Fig. 16. It is important to note that the input voltage and the output resistance are held fixed for these measurements. Therefore, as the conversion ratio is varied, the processed power is also varied.

C. Interleaved Operation

Significant reduction in the input current and output voltage ripples may be achieved through operating the TMMC under the interleaved mode. The two-level TMMC has been investigated under interleaved operation by phase-shifting module [1, 2]'s gating signal 180° from the other two modules. This is the optimized interleaving scheme for the two-level TMMC as it results in optimally minimized input current and output voltage ripples.

The converter is tested at the same operating point as the noninterleaved experiment presented in Section VI-A. The corresponding duty cycle and PWM carrier signals under interleaved operation are shown in Fig. 17(a). The measured voltage and current ripples of the interleaved TMMC are tabulated in Table IV. It is noted that the experimentally measured output voltage and input current ripples are reduced by 38% and 49% as compared to the noninterleaved results (see Table III). The converter's power conversion efficiency is also increased to 96.2% from 95.9%. The simulated non-interleaved and interleaved output voltage and input current waveforms are overlaid on top of each other in Fig. 17(b). For the non-interleaved case, the input current displays a pulsed characteristic. In contrast, for the interleaved case, the input current remains near its average value with the exception of brief, reduced amplitude pulses. The duration of the current pulses is given by the deviation of the first row duty cycles from 50%. As may be observed, the peak-to-peak current ripple is reduced by 52%, however, the rms ripple current is reduced by a much greater factor if the first row modules are operated at a duty cycle near 50%.

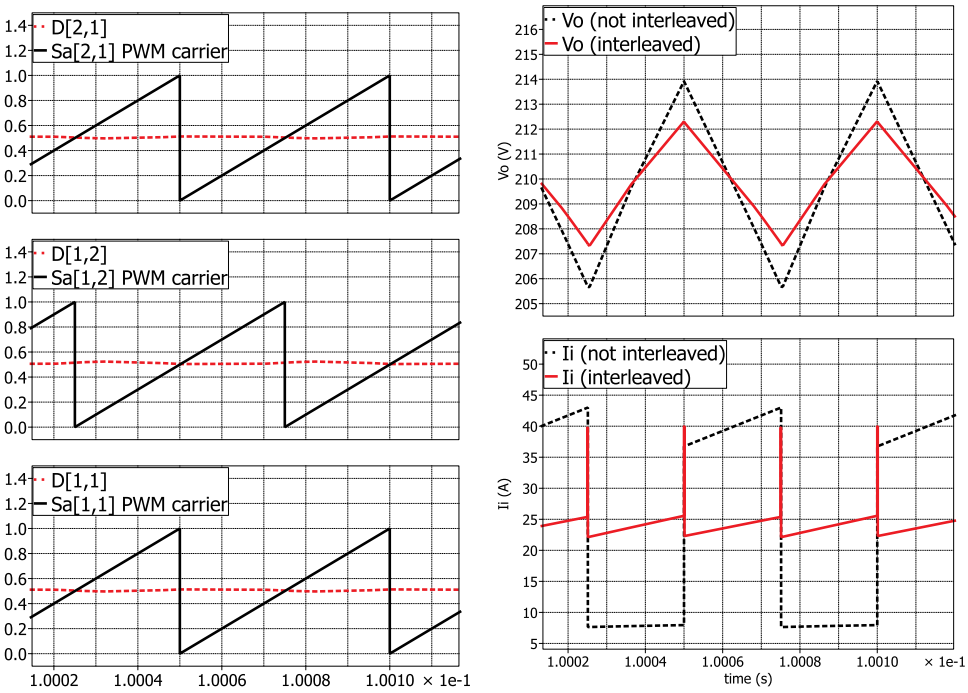


Fig. 17. Simulated interleaved operation results. (a) Duty cycle and PWM carrier signals of the interleaved operation. (b) Simulated ripple comparison between noninterleaved and interleaved operations [input filter capacitors, $C_{\mathrm{LV}[1,j]}$, are neglected to obtain the input current waveforms—See Fig. 11(a)].

As an in-depth analysis of the TMMC is required to identify the optimal interleaving scheme for the n-level topology, it is outside the scope of this paper.

D. Dynamic Operation

The two-level TMMC's dynamic step response is investigated through a 20% output voltage step from 185 to 222 V with an input voltage of 64 V. An output load of 34.8 Ω is selected such that the output power is stepped from 0.98 to 1.42 kW. The simulation and experimental results of this test are shown in Fig. 18. As predicted in Section IV, similar dynamic behavior is observed on the capacitor voltages. Close agreement between experimental and simulations results is also observed. Slightly lower damping is noted in the experimental system as compared to the simulation system.

VII. TMMC as a Multiple-Input Multiple-Output Converter

Due to the TMMC's modular structure, fixed controllable dc voltage nodes are provided above each row. These nodes may be utilized as either inputs or outputs. This is a great advantage of the proposed topology as it may be utilized as an overall power system architecture, providing power to multiple loads at different voltage ratings employing multiple sources at different voltage ratings. The voltages at these nodes are fully controllable in that they need not be integer multiples of the input voltages nor the neighboring rows' capacitor voltages.

An example illustrating the application of the three-level TMMC as a single-input multiple-output converter in step-down mode is shown in Fig. 19. Arbitrary conversion ratios are selected to highlight that integer-multiple conversion ratios between different voltage nodes are not required. As mentioned previously, in step-down only applications, the modules could simply be comprised of a low-side diode and a high-side active switch.

Another advantage which arises from this multiple-node capability of the TMMC is the input voltage modularity which is applicable in step-up operations (see Fig. 20). The input voltage is not restricted to be applied at the input of the first row modules. For applications in which the modules are rated at a lower voltage than the input voltage, the input source may be applied to a row above the first row such that the modules' capacitors do not exceed their rated voltage. This implies that the range of input voltages that may be applied to the TMMC may exceed the rated voltage of available semiconductor technology. Fig. 20 demonstrates the input voltage modularity of the three-

TABLE IV
Ripple Measurements of the Interleaved Two-Level TMMC
($V_i = 70$ V, $V_o/V_i = 3$, $R_o = 26.9$ Ω)

	Simulated	**Experimental**	**% Reduction (experiment)**
ΔV_o (V)	4.9	4.6	40%
ΔI_i (A)	17.6	17.2	52%
$\Delta V_{C[2]}$ (V)	3.3	3.3	0%
$\Delta V_{C[1]}$ (V)	1.7	1.6	66%
$\Delta I_{L[2]}$ (A)	3.3	4.0	0%
$\Delta I_{L[1]}$ (A)	3.3	3.6	5.3%

See Table III for non-interleaved results.

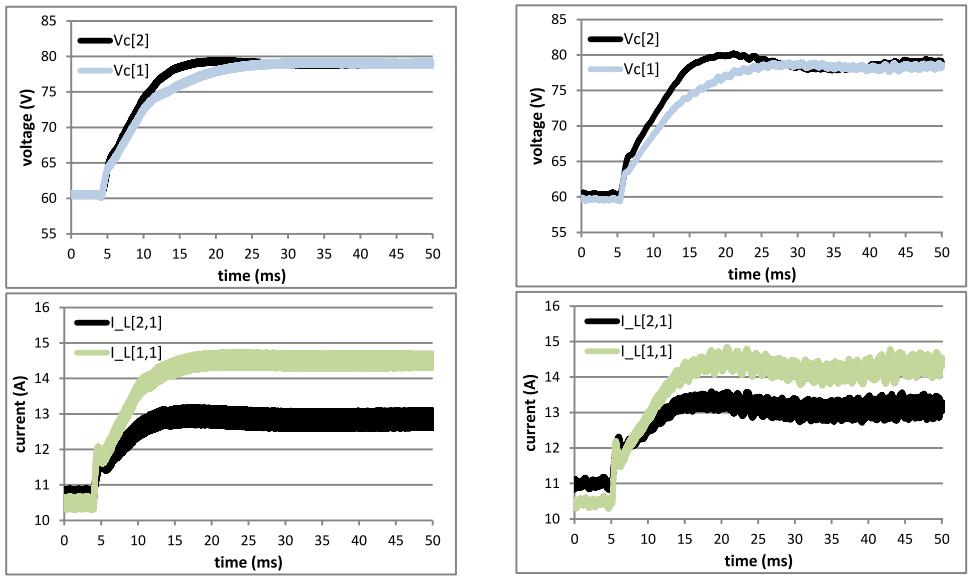


Fig. 18. Dynamic step response of the two-level TMMC of Table II with V_i at 64 V and V_o stepped from 185 to 222 V with a 34.8-Ω load. (a) Simulation results. (b) Experimental results.

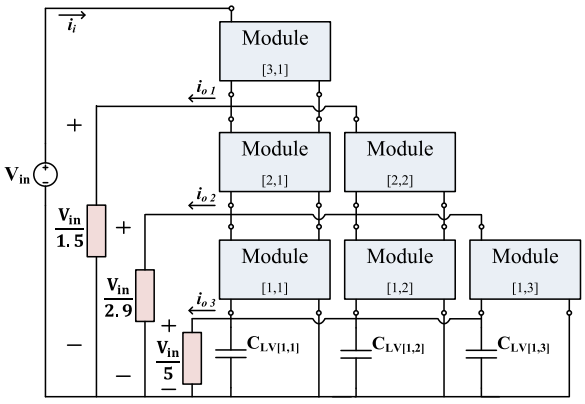


Fig. 19. Three-level step-down TMMC configured as a single-input multiple-output converter.

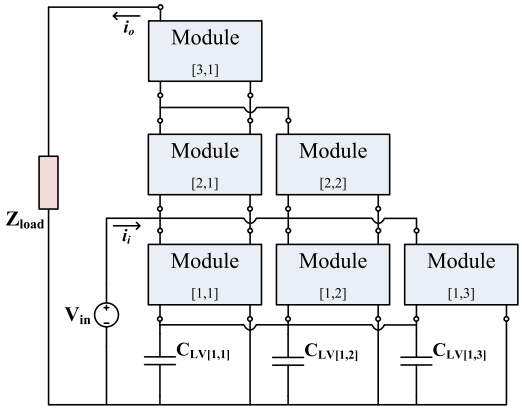


Fig. 20. Three-level step-up TMMC demonstrating input voltage modularity through connection of the input source above the first row.

level TMMC configured as a single-input single-output step-up converter. In the case shown, the input source is applied above the first row.

Through incorporation of multiple inputs and outputs, the power stress to modules at different rows would now vary, and therefore, the power sharing capability of the converter under such applications would lead to a non-triangular structure.

VIII. Conclusion

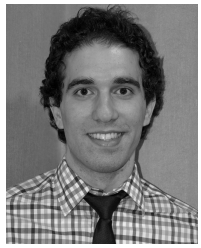
In this paper, a bidirectional modular multilevel dc–dc converter topology and its corresponding control algorithm is proposed. The proposed TMMC converter is capable of equal power sharing among its modules over a broad range of conversion ratios. The proposed control algorithm provides localized control of the modules which enhances the dynamic performance and design flexibility of the converter. The steady-state equations provided in Section V may be utilized for component selection and analysis of the TMMC under non-interleaved operation. Applicability of the topology is experimentally validated through a 1.7-kW implementation of the two-level TMMC with measured efficiencies of 95.9% and 96.2% in step-up and step-down operations, respectively. Through interleaved operation, the output voltage and input current ripples of the TMMC are shown to achieve a reduction of 38% and 49%, respectively. Since each row of the TMMC provides a potential input or output node at a controllable voltage level, multiple-input multiple-output power transfer is readily achievable.

References

[1] F. Khan and L. Tolbert, "A multilevel modular capacitor-clamped dc–dc converter," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1628–1638, Nov. 2007.

[2] F. Khan and L. Tolbert, "Bi-directional power management and fault tolerant feature in a 5-kW multilevel dc-dc converter with modular architecture," *IET Power Electron.*, vol. 2, no. 5, pp. 595–604, 2009.

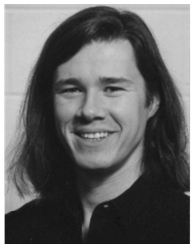
[3] F. Khan and L. Tolbert, "A 5 kW bi-directional multilevel modular dc-dc converter (MMCCC) featuring built in power management for fuel cell and hybrid electric automobiles," in *Proc. IEEE Veh. Power Propuls. Conf.*, 2007, pp. 208–214.
[4] F. Khan and L. Tolbert, "Multiple load-source integration in a multilevel modular capacitor clamped dc-dc converter featuring fault tolerant capability," in *Proc. IEEE 22nd Annu. Appl. Power Electron. Conf.*, 2007, pp. 361–367.
[5] F. Khan, L. Tolbert, and W. Webb, "Start-up and dynamic modeling of the multilevel modular capacitor-clamped converter," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 519–531, Feb. 2010.
[6] D. Cao and F. Z. Peng, "Zero-current-switching multilevel modular switched-capacitor dc-dc converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 3516–3522.
[7] D. Cao, X. Lu, X. Yu, and F. Z. Peng, "Zero voltage switching double-wing multilevel modular switched-capacitor dc-dc converter with voltage regulation," in *Proc. IEEE 28th Annu. Appl. Power Electron. Conf. Expo.*, 2013, pp. 2029–2036.
[8] D. Cao, S. Jiang, and F. Z. Peng, "Optimal design of a multilevel modular capacitor-clamped dc-dc converter," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3816–3826, Aug. 2013.
[9] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," presented at the IEEE Power Tech Conf., Bologna, Italy, 2003, vol. 3.
[10] J. Ferreira, "The multilevel modular DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.
[11] G. J. Kish and P. W. Lehn, "A modular bidirectional DC power flow controller with fault blocking capability for DC networks," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, Jun. 2013, pp. 1–7.
[12] A. Schön and M.-M. Bakran, "A new HVDC-DC converter for the efficient connection of HVDC networks," in *Proc. PCIM Eur. Conf.*, May 2013, pp. 525–532.
[13] S. Manias and G. Kostakis, "A modular dc-dc converter for high output voltage applications," in *Proc. Athens Power Tech, Joint Int. Power Conf.*, 1993, vol. 1, pp. 84–91.
[14] A. Bhinge, N. Mohan, R. Giri, and R. Ayyanar, "Series-parallel connection of dc-dc converter modules with active sharing of input voltage and load current," in *Proc. IEEE 17th Annu. Appl. Power Electron. Conf. Expo.*, 2002, vol. 2, pp. 648–653.
[15] R. Giri, R. Ayyanar, and E. Ledezma, "Input-series and output-series connected modular dc-dc converters with active input voltage and output voltage sharing," in *Proc. IEEE 19th Annu. Appl. Power Electron. Conf. Expo.*, 2004, vol. 3, pp. 1751–1756.
[16] V. Choudhary, E. Ledezma, R. Ayyanar, and R. Button, "Fault tolerant circuit topology and control method for input-series and output-parallel modular dc-dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 402–411, Jan. 2008.
[17] L. Palma and P. Enjeti, "A modular fuel cell, modular dc-dc converter concept for high performance and enhanced reliability," in *Proc. IEEE Power Electron. Spec. Conf.*, 2007, pp. 2633–2638.
[18] D. Montesinos-Miracle, M. Massot-Campos, J. Bergas-Jane, S. Galceran-Arellano, and A. Rufer, "Design and control of a modular multilevel dc/dc converter for regenerative applications," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3970–3979, Aug. 2013.
[19] A. Hagar and P. Lehn, "Comparative evaluation of a new family of transformerless modular dc-dc converters for high-power applications," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 444–452, Feb. 2014.
[20] T. Soong and P. Lehn, "A transformerless high boost dc-dc converter for use in medium/high voltage applications," in *Proc. IEEE 38th Annu. Conf. Ind. Electron. Soc.*, 2012, pp. 174–179.
[21] K. Filsoof and P. Lehn, "Design and control of a bidirectional triangular modular multilevel dc-dc converter," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, Jun. 2013, pp. 1–7.
[22] G. L. Brainard, "Non-dissipative battery charger equalizer," U.S. Patent 5 479 083, Dec. 26, 1995.
[23] G. Walker and J. Pierce, "Photovoltaic dc-dc module integrated converter for novel cascaded and bypass grid connection topologies—Design and optimisation," in *Proc. IEEE 37th Power Electron. Spec. Conf.*, 2006, pp. 1–7.
[24] H. Bergveld, D. Buthker, C. Castello, T. Doorn, A. de Jong, R. van Otten, and K. de Waal, "Module-level dc/dc conversion for photovoltaic systems: The delta-conversion concept," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 2005–2013, Apr. 2013.
[25] M. Zaman, S. Poshtkouhi, V. Palaniappan, K. Li, H. Bergveld, S. Myskorg, and O. Trescases, "Distributed power-management architecture for a low-profile concentrating-PV system," in *Proc. 15th Int. Power Electron. Motion Control Conf.*, 2012, pp. LS2d.4-1–LS2d.4-8.
[26] P. Shenoy, K. Kim, B. Johnson, and P. Krein, "Differential power processing for increased energy production and reliability of photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2968–2979, Jun. 2013.
[27] C. Schaef and J. Stauth, "Multilevel power-point-tracking for variable-conversion-ratio photovoltaic ladder converters," in *Proc. IEEE 14th Workshop Control Model. Power Electron.*, Jun. 2013, pp. 1–7.
[28] P. S. Shenoy and P. T. Krein, "Differential power processing for dc systems," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1795–1806, Apr. 2013.
[29] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Norwell, MA, USA: Kluwer, 2001.
[30] D. Graovac, M. Pürschel, and A. Kiep, *MOSFET Power Losses Calculation Using the Data-Sheet Parameters*, Infineon Technologies, Neubiberg, Germany, 2006.
[31] *PLECS User Manual Version 3.5*, Plexim, Zurich, Switzerland, 2014.



Kia Filsoof (S'08) received the B.A.Sc. degree in electronics engineering from Simon Fraser University, Burnaby, BC, Canada, in 2011. He is currently working toward the Ph.D. degree in electrical engineering at the University of Toronto, Toronto, ON, Canada.

His research interests include design, modeling, control, and experimental implementation of power converters for a wide range of applications. He is also interested in analog circuit design for signal processing applications.

Mr. Filsoof is a Member of the IEEE Power Electronics Society and the IEEE Industrial Electronics Society. He received the Ontario Graduate Scholarship Award in 2012.



Peter W. Lehn (SM'05) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Manitoba, Winnipeg, MB, Canada, in 1990 and 1992, respectively, and the Ph.D. degree from the University of Toronto, Toronto, ON, Canada, in 1999.

He joined the faculty at the University of Toronto in 1999. He spent six months as a Visiting Professor at the University of Erlangen-Nuremberg in 2001. His research interests include HVDC technologies, grid integration of solar and wind energy systems, as well as both theoretical and experimental analysis of power electronics.

Dr. Lehn is currently an Editor of the IEEE TRANSACTIONS ON ENERGY CONVERSION and the Chair of the IEEE Working Group on Distributed Resources.