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Analysis and implementation of a new single-switch buck–boost DC/DC converter

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Abstract: In this study, a novel buck–boost DC/DC converter is presented. The circuit structure of the proposed converter consists of a single power switch, two diodes and some energy storage elements. Employing only a single power switch reduces the implementation cost and switching power losses. The proposed converter has higher voltage gain in step-up mode in comparison with conventional buck–boost and Cuk converter. In addition, this converter expands the continuous conduction mode (CCM) operational region. The presented converter has three operation modes in CCM. The second mode reduces the voltage stresses across the capacitors. Therefore the current stresses on diodes are also reduced. To verify the operation of the proposed converter, the experimental results are provided using a hardware prototype.

1 Introduction

Recently, DC/DC converters have attracted great attention by researchers. Voltage bucking/boosting is required in many applications such as fuel-cell systems [1–4], portable devices such as notebooks and mobile phones, light-emitting diode products and car electronic devices [5–7]. Owing to fluctuations in the output voltage of the battery systems, an additional DC/DC buck–boost converter is needed to regulate the output voltage. Several converter types are capable of providing both step-up and step-down voltage conversion including the inverting buck–boost converter [8, 9], the flyback converter, the Cuk converter and the single-ended primary-inductance converter (SEPIC) [10]. However, these converters greatly stress the switches. The flyback converter has a high-leakage inductance and its efficiency is low [11]. Some DC/DC buck–boost converters are recently presented by using the KY converters [12–15]. However, four power switches have been used in these converters. In [16], a buck–boost converter combining KY and buck converter has been presented to reduce the number of power switches to two, but the maximum voltage gain of all these buck–boost converters is two. KY converters are also used to construct high step-up converters like in [17]. In [18], a non-inverting buck–boost converter for fuel-cell system using three power switches is proposed with a voltage gain equal to the proposed converter in this paper. The main disadvantage of the KY converters is that some capacitors are suddenly charged in some operational modes. As a result, current stresses on diodes, switches and capacitors are intensified. This problem causes some implementation difficulties.

In this paper, a new buck–boost converter is proposed. The voltage gain of the proposed converter in step-up mode is higher than the basic non-isolated buck–boost converters such as traditional buck–boost, Cuk, Zeta and SEPIC. The presented converter operates in three modes in continuous conduction mode (CCM). The second mode of KY converters in which the power switch is turned off, is divided into two modes in the proposed converter. These two modes do not allow the capacitors to be parallel suddenly unlike KY converters. Therefore the proposed converter solves the aforementioned problem of KY converters which causes the stresses on the components of the circuit to be reduced. In this topology, only one power switch is used which makes the control scheme simple as well as reducing the switching power losses. Moreover, CCM operational region is broadened in the proposed converter in comparison with the Cuk converter. Experimental results are provided to verify the feasibility of the proposed converter.

2 Proposed converter structure

The circuit configuration of the presented converter is shown in Fig. 1. As shown in Fig. 1, the proposed converter consists of three capacitors, two inductors, one power switch and two diodes. Capacitors C_1 and C_2 are in parallel by two diodes. Their voltages are both $D/(1-D)$ times of the input voltage. The voltage of the capacitor C_3 is also determined by the capacitor C_1 and the input voltage which is also $D/(1-D)$ times of the input voltage. The load is connected in parallel with capacitors C_2 and C_3. Therefore the output load voltage will be $2D/(1-D)$ times of the input voltage.

The proposed converter operates in three modes in CCM. First mode occurs when the power switch is on and other two modes occur when the power switch is off. Last two modes cause stresses on diodes and capacitors to be reduced while KY converters have two modes that stress

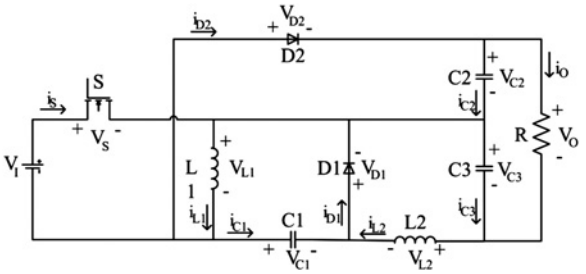

Fig. 1 *Circuit configuration of the proposed converter*

capacitors, switches and diodes. The proposed converter operates in five modes in discontinuous conduction mode (DCM).

3 Operating principles of the proposed converter

To simplify the analysis, the below assumptions are considered.

(1) All the capacitors are large enough. Hence, the voltage ripples of capacitors are neglected to obtain the voltage gain in steady-state operation.
(2) The power switches are ideal, and the parasitic capacitor of the power switch is neglected.

The steady-state analysis of the proposed converter in CCM and DCM are explained in the following sections.

3.1 CCM operation

The typical waveforms of the proposed converter in CCM are depicted in Fig. 2*a*. The current paths of different modes in CCM operation are also shown in Fig. 3.

3.1.1 Mode I: During the time interval $[t_0, t_1]$, the switch (S) is turned on and the diodes (D_1, D_2) are turned off. As seen in Fig. 3*a*, the inductor L_1 is energised via input voltage. As it is shown in Fig. 2*a*, the inductors L_2 is also linearly magnetised by capacitors C_1, C_3 and the input voltage. Besides, the energy stored in the capacitors C_2 and C_3 are discharged to the load. Thus, the following equations can be achieved

$$V_{L_1} = V_I \tag{1}$$

$$V_{L_2} = V_I + V_{C_1} - V_{C_3} \tag{2}$$

3.1.2 Mode II: During the time interval $[t_1, t_2]$, S is turned off and D_1 is turned on and D_2 is still turned off. As seen in Fig. 3*b*, the capacitors C_1 and C_3 are charged via inductors L_1 and L_2, respectively. All of inductors are demagnetised linearly. Also, the energy stored in capacitor C_2 is discharged to the load. Thus, the following equations can

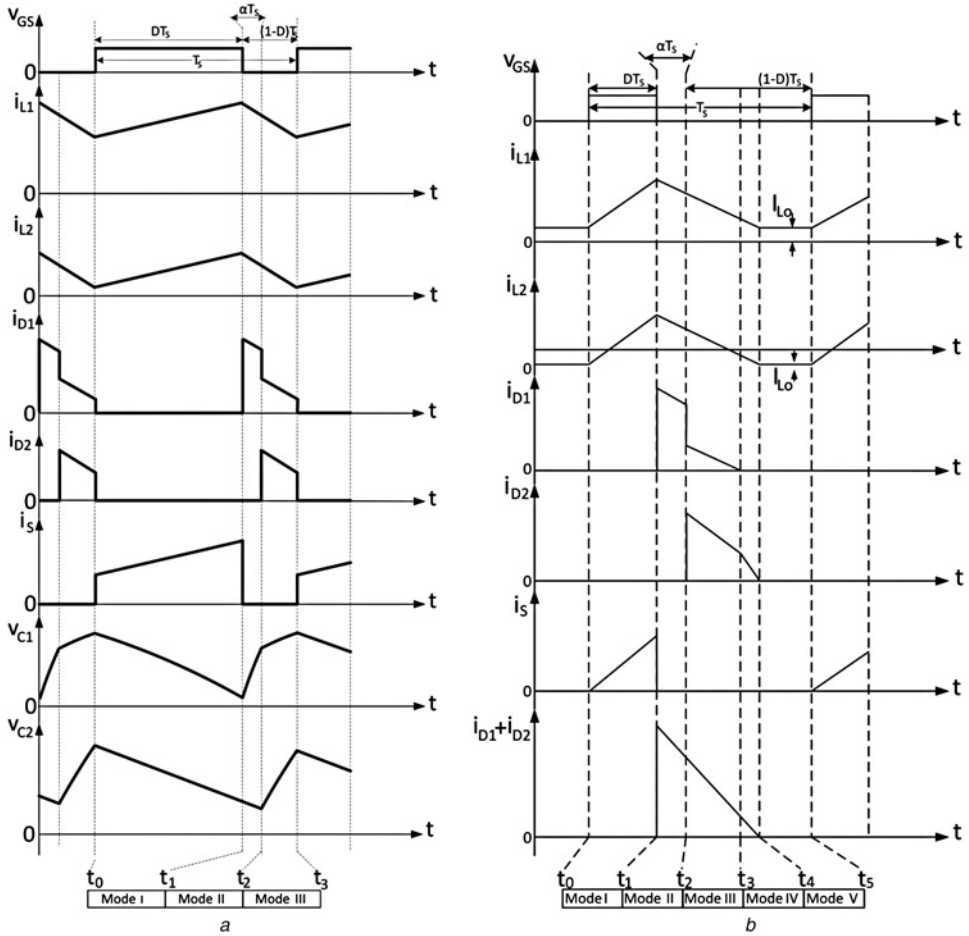

Fig. 2 *Typical waveforms of the proposed converter*
a CCM operation
b DCM operation

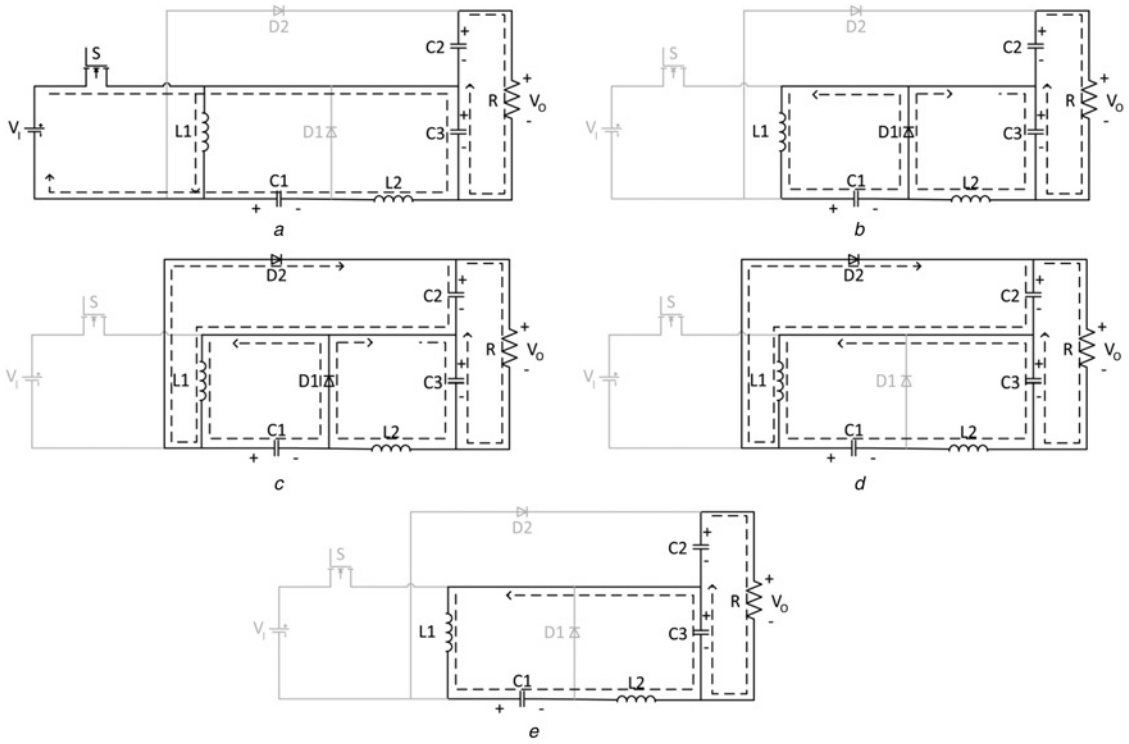

Fig. 3 *Current flow path of the proposed converter in CCM operation*

a Mode I
b Mode II
c Mode III
d Mode IV (in DCM)
e Mode V (in DCM)

be achieved

$$V_{L_1} = -V_{C_1} \tag{3}$$

$$V_{L_2} = -V_{C_3} \tag{4}$$

Capacitors C_1 and C_2 are charged and discharged, respectively, until their voltages become equal. At this moment the second mode is finished. This mode prevents the capacitors C_1 and C_2 to be parallel suddenly with different voltages. Therefore the current spikes through diodes and capacitors are avoided.

3.1.3 Mode III: During the time interval $[t_2, t_3]$, S is still turned off. The voltages of the capacitors C_1 and C_2 are equal, so D_2 is turned on as well as D_1. The current flow path is shown in Fig. 3*c*. As the voltages of capacitors C_1 and C_2 are the same, the voltage across D_2 becomes zero and after a moment it is changed to positive. Therefore D_2 can be turned on. Then, capacitors C_1 and C_2 are in parallel. It is shown in Fig. 2*a* that the voltages of capacitors C_1 and C_2 are the same. The capacitors C_1 and C_2 are charged by the inductor L_1. Also, the inductor L_2 charges the capacitor C_3. All of the inductors are demagnetised linearly at this mode. Hence, the following equations can be earned

$$V_{L_1} = -V_{C_1} \tag{5}$$

$$V_{L_2} = -V_{C_3} \tag{6}$$

During this mode, capacitors C_1 and C_2 are in parallel. Besides, it is assumed that the voltages of capacitors are constant. Thus, the following equation can be considered

$$V_{C_1} = V_{C_2} \tag{7}$$

By applying the volt–second balance principle on L_1 and using (1), (3) and (5), the following equation is obtained as

$$\langle V_{L_1} \rangle = DV_I + \alpha\left(-V_{C_1}\right) + (1 - D - \alpha)\left(-V_{C_1}\right) = 0 \tag{8}$$

where αT_s is the time interval of the second mode. By simplifying (8), the following equation can be expressed as

$$V_{C_1} = V_{C_2} = \frac{D}{1 - D} V_I \tag{9}$$

Sequentially, using the voltage–second balance on L_2, the following equations can be achieved as

$$\langle V_{L_2} \rangle = D\left(V_I + V_{C_1} - V_{C_3}\right) + \alpha\left(-V_{C_3}\right) + (1 - D - \alpha) \times \left(-V_{C_3}\right) = 0 \tag{10}$$

$$V_{C_3} = \frac{D}{1 - D} V_I \tag{11}$$

$$V_{\mathrm{O}} = V_{C_2} + V_{C_3} \tag{12}$$

Substituting (9) and (11) into (12), the CCM voltage gain is

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derived as follows

$$G_{(V)\mathrm{CCM}} = \frac{2D}{1-D} \tag{13}$$

According to Fig. 3, the currents which flow through capacitors C_1 and C_2 can be written as

$$i_{C_1} = \begin{cases} -I_{L_2}, & 0 < t < DT \\ I_{L_1}, & DT < t < (\alpha + D)T \\ \dfrac{C1}{C1 + C2}\left(I_{L_1} - I_{\mathrm{O}}\right), & (\alpha + D)T < t < T \end{cases} \tag{14}$$

$$i_{C_2} = \begin{cases} -I_{\mathrm{O}}, & 0 < t < DT \\ -I_{\mathrm{O}}, & DT < t < (\alpha + D)T \\ \dfrac{C_2}{C_1 + C_2}\left(I_{L_1} - I_{\mathrm{O}}\right), & (\alpha + D)T < t < T \end{cases} \tag{15}$$

By applying the ampere–second balance for capacitors C_1 and C_2 and using (14), (15), the following equations are derived as

$$\langle i_{C_1} \rangle = -DI_{L_2} + \alpha I_{L_1} + (1 - \alpha - D)\frac{C_1}{C_1 + C_2}\left(I_{L_1} - I_{\mathrm{o}}\right) = 0 \tag{16}$$

$$\langle i_{C_2} \rangle = -(D + \alpha)I_{\mathrm{o}} + (1 - \alpha - D)\frac{C_2}{C_1 + C_2}\left(I_{L_1} - I_{\mathrm{o}}\right) = 0 \tag{17}$$

Moreover, the average current of L_2 is approximated by the output current.

$$I_{L_2} \cong I_{\mathrm{O}} \tag{18}$$

The current gain in CCM can be obtained as follows

$$G_{(I)\mathrm{CCM}} = \frac{1-D}{2D} \tag{19}$$

By simplifying the (16)–(19), α is derived as follows

$$\alpha = \frac{(D - D^2)(C_2 - C_1)}{(C_1 + C_2) + D(C_2 - C_1)} \tag{20}$$

The voltage gain curves for the proposed converter and Cuk converter in CCM operation are plotted in Fig. 4. It is seen that the voltage gain of the proposed converter in both buck and boost modes is higher than the Cuk converter.

3.2 DCM operation

Operating in DCM, the proposed converter operation can be divided into five modes. The typical waveforms of the proposed converter in DCM are depicted in Fig. 2*b*. The current paths of different modes in DCM operation are also shown in Fig. 3.

3.2.1 Mode I: During the time interval $[t_0, t_1]$, S is turned on and the diodes are turned off. As seen in Fig. 3*a*, this mode of DCM is the same as the first mode of CCM operation. Therefore (1) and (2) are valid in this mode too.

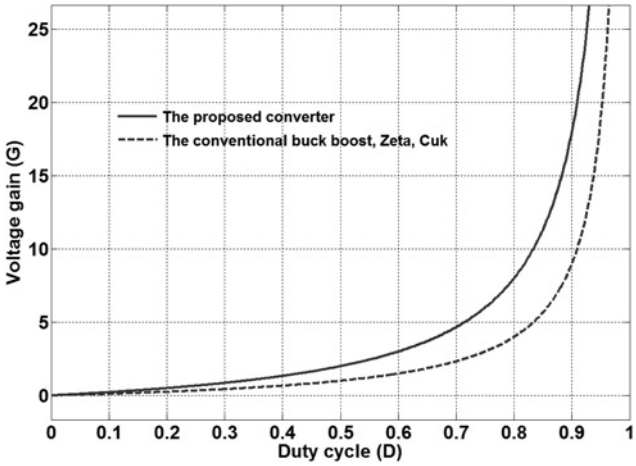

Fig. 4 *Voltage gains of the proposed converter and Cuk converter in CCM operation*

3.2.2 Mode II: During the time interval $[t_1, t_2]$, S is turned off and D_1 is turned on and D_2 is still off. As seen in Fig. 3*b*, this mode of DCM is the same as the second mode of CCM operation and as a result, (3) and (4) are valid in this mode too.

3.2.3 Mode III: During the time interval $[t_2, t_3]$, S still is turned off and D_1 and D_2 are turned on. As seen in Fig. 3*c*, this mode of DCM is the same as the third mode of CCM operation. Therefore (5) and (6) are valid in this mode too.

3.2.4 Mode IV: During the time interval $[t_3, t_4]$, the switch is still off and the diode D_1 is turned off and the diode D_2 is remained on. Equations (5) and (6) are still valid in this mode too. The current flow path is shown in Fig. 3*d*.

3.2.5 Mode V: During the time interval $[t_4, t_5]$, the switch and the diodes are turned off. The currents of the inductors will be constant in this mode. Consequently, the voltages across the inductors are nulls: $v_{L1} = v_{L2} = 0$ [11]. The current flow path is shown in Fig. 3*e*.

By applying the volt–second balance principle on L_1 and using (1), (3) and (5), the following equation is obtained as

$$\langle V_{L_1} \rangle = DV_I - (\alpha + \beta)V_{C_1} = 0 \tag{21}$$

where βT_s is the time interval of the third and fourth modes in DCM. Thus, by simplifying (21), the following equation can be expressed as

$$V_{C_1} = \frac{D}{\alpha + \beta}V_I \tag{22}$$

Using (22), (7) and (12), the voltage gain in DCM is derived as follows

$$G_{(V)\mathrm{DCM}} = \frac{2D}{\alpha + \beta} \tag{23}$$

The integral form of the current equation of inductor L_1 is as follows

$$i_{L_1}(t) = i_{L_1}(t_0) + \frac{1}{L_1}\int_{t_0}^{t} v_{L_1}\,\mathrm{d}\tau \tag{24}$$

Substituting (1) into (24) and for $t = DT$, $t_0 = 0$, yielding

$$\Delta i_{L_1} = \frac{D(V_I)}{fL_1} \tag{25}$$

The current ripple of the inductor L_2 can be obtained as well

$$\Delta i_{L_2} = \frac{DV_I}{fL_2} \tag{26}$$

According to the waveforms shown in Fig. 2*b*, the average current values can be written as follows

$$I_{L_1} = \frac{D+\alpha+\beta}{2}\Delta i_{L_1} + I_{Lo} \tag{27}$$

$$I_{L_2} = \frac{D+\alpha+\beta}{2}\Delta i_{L_2} + I_{Lo} \tag{28}$$

$$I_I = \frac{D}{2}\left(\Delta i_{L_1} + \Delta i_{L_2}\right) \tag{29}$$

Using (18), (27)–(29) and the current gain in DCM, I_{Lo} is derived as follows

$$I_{Lo} = \frac{V_I D}{f}\left[\left(\left(\frac{D+\alpha+\beta}{2}\right) - \frac{\alpha+\beta}{4}\right)\frac{1}{L_2} - \frac{\alpha+\beta}{4L_1}\right] \tag{30}$$

In DCM operation mode, the currents flowing from inductors do not reach zero. However, they reach to the value I_{Lo} as it is shown in Fig. 2*b*. Substituting (28) and (30) into (18), yielding

$$I_{L_2} = I_o = \frac{V_o}{R} = \frac{V_I D}{fL_2}\left(\frac{D+\alpha+\beta}{2}\right) - \frac{V_I D}{f}\left[\left(\left(\frac{D+\alpha+\beta}{2}\right) - \frac{\alpha+\beta}{4}\right)\frac{1}{L_2} - \frac{\alpha+\beta}{4L_1}\right] \tag{31}$$

$$(\alpha+\beta) = \sqrt{\frac{8f(L_1||L_2)}{R_L}} \tag{32}$$

Using (23) and (32), $G_{(v)\mathrm{DCM}}$ can be expressed in terms of D, R_L, f and L_3 as below

$$G_{(V)\mathrm{DCM}} = \frac{2D}{\sqrt{\frac{8f(L_1||L_2)}{R_L}}} \tag{33}$$

When the average currents of diodes become less than half of the diodes' current ripples, the diodes will be turned off and as a result the proposed converter operates under DCM. The average input current under CCM operation is as follows

$$I_I = D\left(I_{L_1} + I_{L_2}\right) \tag{34}$$

The diodes are turned off simultaneously so that DCM operation criterion is considered for both diodes' current.

$$I_{L_1} + I_{L_2} < \Delta i_{L_1} + \Delta i_{L_2} \tag{35}$$

Substituting current ripples of the inductors from (25) and (26) into (35) and simplifying, which yields to

$$\frac{4f(L_1||L_2)}{R_L} < (\alpha+\beta)^2 \tag{36}$$

Therefore the left hand of the inequality is the normalised inductors time constant. To obtain the boundary normalised inductor time constant more simple, all inductors are considered the same. Therefore the following equation can be achieved

$$\tau_L = \frac{4f(L_1||L_2)}{R_L} \tag{37}$$

Substituting (37) into (33), the voltage gain of DCM can be obtained as

$$G_{(V)\mathrm{DCM}} = \frac{2D}{\sqrt{2\tau_L}} \tag{38}$$

3.3 Boundary operating condition of the proposed converter

In the boundary mode, the voltage gain of CCM equals to the voltage gain of DCM. From (13) and (38), the boundary normalised inductor time constant $\tau_{L,\mathrm{B}}$ can be given as follows

$$\tau_{L,\mathrm{B}} = \left(\frac{1}{2}\right)(1-D)^2 \tag{39}$$

The curve of $\tau_{L,\mathrm{B}}$ is indicated in Fig. 5. If τ_L is larger than $\tau_{L,\mathrm{B}}$, the proposed converter operates in CCM.

4 Voltage stresses and efficiency analysis

Voltage stresses on different components of the circuit are the most important criteria to choose the appropriate devices. The voltage ripple across the capacitors are neglected to simplify the voltage stress analysis on the components of the proposed converter. The maximum peak voltages of the switch S_1 and

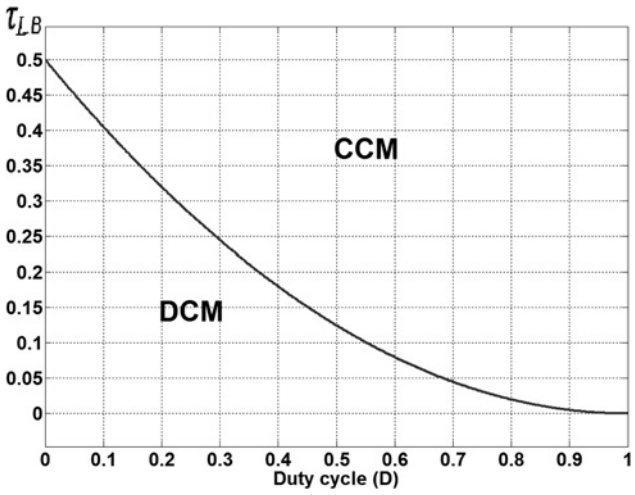

Fig. 5 *Boundary condition of the proposed converter*

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diodes D_1 and D_2 at the steady state are

$$V_S = V_I + V_{C_1} = \frac{1}{1-D} V_I \tag{40}$$

$$V_{D_1} = V_I + V_{C_1} = \frac{1}{1-D} V_I \tag{41}$$

$$V_{D_2} = V_I + V_{C_2} = \frac{1}{1-D} V_I \tag{42}$$

The voltage stress on the switching device is compared with the voltage stress on the switch of conventional buck–boost, Zeta and Cuk converters. It is also compared with the KY buck–boost [i.e. two-dimensional (2D) converter] [12]. The voltage stress on the switch of the presented converter with respect to the voltage gain is as follows

$$V_S = \frac{G+2}{2} V_I \tag{43}$$

The voltage stress on the switch of the conventional buck–boost, Zeta and Cuk converters with respect to the voltage gain are as follows

$$V_S = (G+1) V_I \tag{44}$$

The voltage stress on the switch of the KY buck–boost (i.e. 2D converter) with respect to the voltage gain is as follows

$$V_S = V_I \tag{45}$$

There are two switches in the KY buck–boost converter structure. Therefore the total voltage stress will be

$$PIV_{\text{total}} = 2V_I \tag{46}$$

The comparison of the voltage stresses of the different converters are depicted in Fig. 6. As it is shown, the voltage stress of the switch in the presented converter is less than other converters. It is worth noting that the maximum gain of the KY converter is two.

An equivalent circuit of the proposed converter with parasitic resistances is shown in Fig. 7. In this figure, r_{DS1} is the metal-oxide semiconductor field-effect transistors' (MOSFETs) on-resistances, r_{D_1} and r_{D_2} are the diodes' forward resistances, V_{F1} and V_{F2} are the diodes' threshold voltages, r_{L_1} and r_{L_2} are the equivalent series resistances (ESRs) of inductors L_1 and L_2 and r_{c_1}, r_{c_2} and r_{c_3} are the ESR of capacitors C_1, C_2 and C_3, respectively. To simplify the equations, the capacitors C_1 and C_2 are considered the same. Therefore the time duration of the second mode in CCM is neglect able ($\alpha = 0$). The voltage and current ripples across the capacitors and inductors are ignored, respectively. The root-mean-square (rms) values of inductor currents can be calculated as follows

$$I_{L_1} = \frac{1+D}{1-D} I_o \tag{47}$$

$$I_{L_2} = I_o \tag{48}$$

The conduction losses of inductors L_1 and L_2 are

$$P_{rL_1} = \frac{rL_1(1+D)^2 P_o}{(1-D)^2 R_L} \tag{49}$$

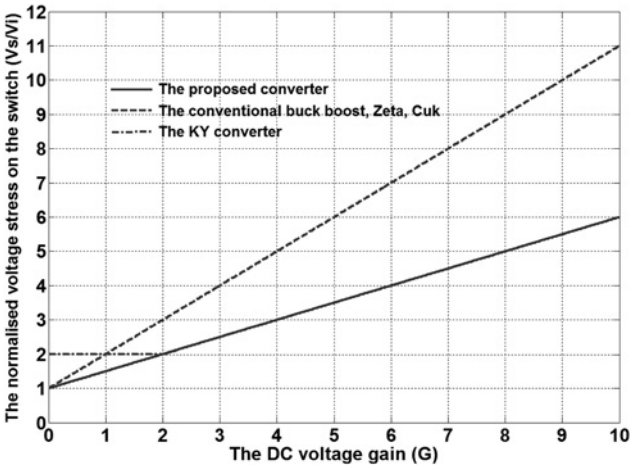

Fig. 6 *Voltage stress comparison of the different converters*

$$P_{rL_2} = \frac{rL_2 P_o}{R_L} \tag{50}$$

The current flowing from the switch and its rms value can be given as

$$i_S = \begin{cases} I_{L_1} + I_{L_2}, & 0 < t < DT \\ 0, & DT < t < T \end{cases} \tag{51}$$

$$i_S = \sqrt{\frac{1}{T}\int_0^{DT} \left(I_{L_1} + I_{L_2}\right)^2 \mathrm{d}t} = \frac{2\sqrt{D} I_o}{1-D} \tag{52}$$

The conduction loss of the power switch is

$$P_{r\text{DS}} = \frac{4Dr_{\text{DS}} P_o}{(1-D)^2 R_L} \tag{53}$$

According to (14) and (15), the rms value of the capacitors currents C_1 and C_2 can be written as

$$i_{C_1\text{rms}} = i_{C_2\text{rms}} = I_o \sqrt{\frac{D}{1-D}} \tag{54}$$

The power losses in capacitors C_1 and C_2 are

$$P_{rC_1} = P_{rC_2} = \frac{r_C D P_o}{(1-D) R_L} \tag{55}$$

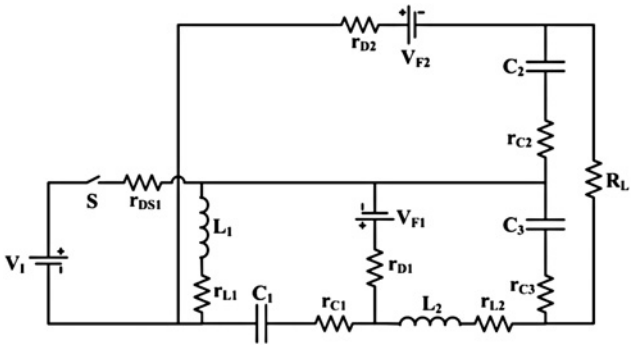

Fig. 7 *Equivalent circuit of proposed converter with parasitic resistances and diode forward conducting voltage*

The current flowing through the capacitor C_3 and its rms value can be given as follows

$$i_{C_3} = \begin{cases} \dfrac{\Delta i_{L_2} t}{DT} - \dfrac{\Delta i_{L_2}}{2}, & 0 < t < DT \\ \dfrac{-\Delta i_{L_2}(t - DT)}{(1-D)T} + \dfrac{\Delta i_{L_2}}{2}, & DT < t < T \end{cases} \tag{56}$$

$$i_{C_3\text{rms}} = \frac{R_L(1-D)I_\text{o}}{\sqrt{12} f_s L_2} \tag{57}$$

The power losses in capacitor C_3 is

$$P_{rC_3} = \frac{r_{C_3}(1-D)^2 R_L P_\text{o}}{12 f_s L_2^2} \tag{58}$$

Similarly, the diodes currents and their rms value can be written as

$$i_{\text{D}_1} = \begin{cases} 0, & 0 < t < DT \\ \dfrac{1}{1-D} I_\text{o}, & DT < t < T \end{cases} \tag{59}$$

$$i_{\text{D}_2} = \begin{cases} 0, & 0 < t < DT \\ \dfrac{D}{1-D} I_\text{o}, & DT < t < T \end{cases} \tag{60}$$

$$i_{\text{D}_1\text{rms}} = \sqrt{\frac{1}{T}\int_{DT}^{T} \left(\frac{I_\text{o}}{1-D}\right)^2 \text{d}t} = \frac{I_\text{o}}{\sqrt{1-D}} \tag{61}$$

$$i_{\text{D}_2\text{rms}} = \sqrt{\frac{1}{T}\int_{DT}^{T} \left(\frac{I_\text{o}}{1-D}\right)^2 {I_\text{o}}^2 \text{d}t} = \frac{\sqrt{D}}{\sqrt{1-D}} \tag{62}$$

The conduction losses of the diodes can be calculated as

$$P_{r\text{D}_1} = \frac{r_{\text{D}_1} P_\text{o}}{(1-D)R_L} \tag{63}$$

$$P_{r\text{D}_2} = \frac{r_{\text{D}_2} D P_\text{o}}{(1-D)R_L} \tag{64}$$

The average diode currents are also calculated below in order to find the power losses associated with the forward voltages.

$$i_{\text{D}_1\text{avg}} = \frac{1}{T}\int_{DT}^{T} \frac{I_\text{o}}{1-D} \text{d}t = I_\text{o} \tag{65}$$

$$i_{\text{D}_2\text{avg}} = \frac{1}{T}\int_{DT}^{T} \frac{D}{1-D} I_\text{o} \text{d}t = DI_\text{o} \tag{66}$$

$$P_{VF1} = \frac{V_{F1} P_\text{o}}{V_\text{o}} \tag{67}$$

$$P_{VF2} = \frac{V_{F1} D P_\text{o}}{V_\text{o}} \tag{68}$$

The total power loss of the converter can be written as

$$\begin{aligned} P_{\text{Loss-Total}} = {} & P_{rL_1} + P_{rL_2} + P_{rC_1} + P_{rC_2} + P_{rC_3} \\ & + P_{r\text{D}_1} + P_{r\text{D}_2} + P_{VF1} + P_{VF2} + P_{r\text{DS}} \end{aligned} \tag{69}$$

Thus, the efficiency is

$$\eta = \frac{P_\text{o}}{P_\text{o} + P_{\text{Loss-Total}}} \tag{70}$$

Fig. 8 shows the efficiency curve under different load conditions. The parameters given in Table 1 are used to determine the efficiency of the presented converter. It is also considered that r_{DS_1}, r_{D_1} and r_{D_2} are 23 mΩ. Also, r_{L_1}, r_{L_2}, r_{c_1}, r_{c_2} and r_{c_3} are taken to be 11 mΩ. The threshold voltages of the diodes are also considered to be 0.7 V. As it is shown in Fig. 8, the presented converter operates with an acceptable efficiency characteristic under different load conditions. The efficiency of presented converter is compared with the converter presented in [18] in Fig. 8. As it is shown in Fig. 8, the presented converter has higher efficiency.

4.1 Design and experimental results

To verify the operation of the proposed converter, experimental results are provided. Specifications of the implemented circuit are given in Table 1. When τ_L is larger than $\tau_{L,\text{B}}$, the proposed converter operates in CCM. By substituting parameters given in Table 1 into (37) and (39),

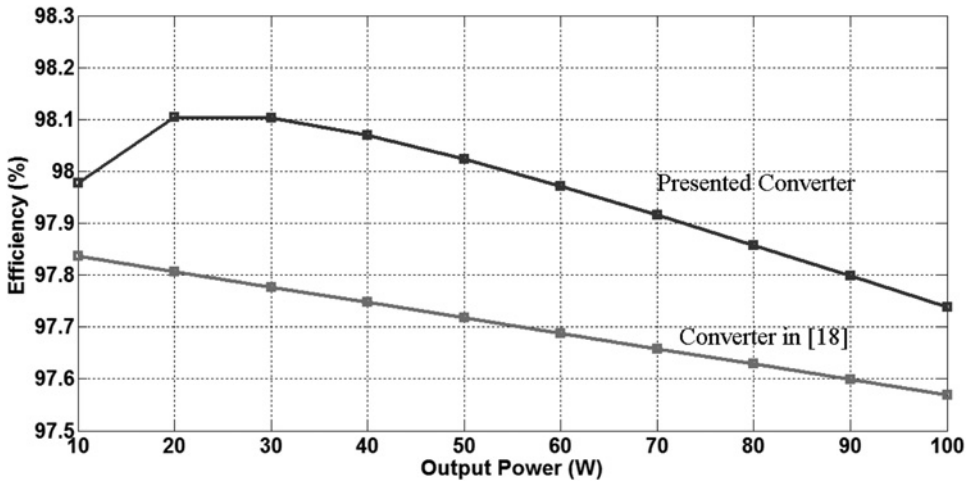

Fig. 8 *Efficiency of the presented converter for various output powers*

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the minimum values of the inductors are found as

$$L_1||L_2 > 69.5\ \mu\text{H} \tag{71}$$

To mitigate the ripple of the output voltage to a tolerant range is main consideration. Hence, the estimated capacitances depend on

$$C_3 \geq \frac{D^2 V_I}{f^2 L_2 V_{r3}} \tag{72}$$

$$C_2 \geq \frac{2D^2}{(1-D)fR_L L_2 V_{r2}} \tag{73}$$

$$C_1 \geq \frac{DV_o}{fR_L V_{r1}} \tag{74}$$

Table 1 Specifications of the implemented prototype

Specifications	Values
input DC voltage	$V_{in} = 15$ V
output DC voltage in CCM	$V_{out} = 50$ V
switching frequency	$F = 30$ kHz, (5 kHz in DCM)
fast diodes D_1, D_2	STTH2002C
inductors L_1/L_2	1.2 mH/970 μH
capacitors C_1, C_2, C_3	100, 630, 100 μF
load	150 Ω
power switch (MOSFET)	IRFP460

where V_{r1-3} are the voltage ripple of the capacitors, respectively. The output voltage ripple is the sum of V_{r2} and V_{r3}. By substituting $V_{r3} = 0.04$, $V_{r2} = 0.01$ and $V_{r1} = 0.05$ into (72)–(74), the minimum values for capacitors are as follows

$$C_1 \geq 89\ \mu\text{F}; \quad C_2 \geq 60\ \mu\text{F}; \quad C_3 \geq 94\ \mu\text{F} \tag{75}$$

Fig. 9 shows the experimental results of the presented converter operating in CCM. Fig. 9*a* shows the pulse which is applied to the switch. The output voltage is also depicted in Fig. 9*b*. As it is shown, the output voltage is 50 V. To measure the currents following from the inductors, a 0.5 Ω resistor is used in series with the inductors. The current waveforms of the inductors L_1 and L_2 are shown in Figs. 9*c* and *d*, respectively. The operation of the proposed converter is also tested in DCM. Fig. 10 shows the experimental results of the presented converter operating in DCM. Fig. 10*a* shows the pulse which is applied to the switch. The output voltage is also depicted in Fig. 10*b*. As it is shown, the output voltage is 20 V. The current waveforms of the inductors L_1 and L_2 are shown in Figs. 10*c* and *d*, respectively. As it is shown in these figures, the currents values are non-zero and the I_{Lo} calculated in (30) is clear. The experimental results validate the operation and analyses of the presented converter in both the CCM and DCM modes.

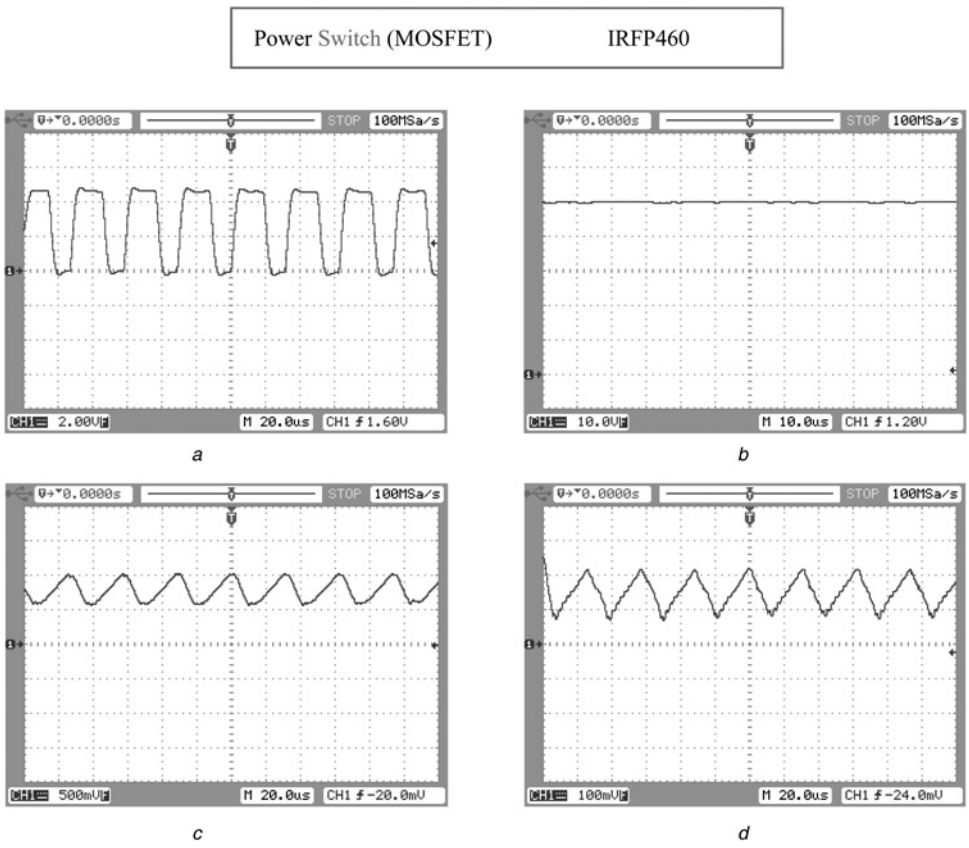

Fig. 9 *Typical waveforms in CCM*

a Duty cycle (D)
b Output voltage and its ripple
c Current of inductor L_1 (i_{L_1})
d Current of inductor L_2 (i_{L_2})

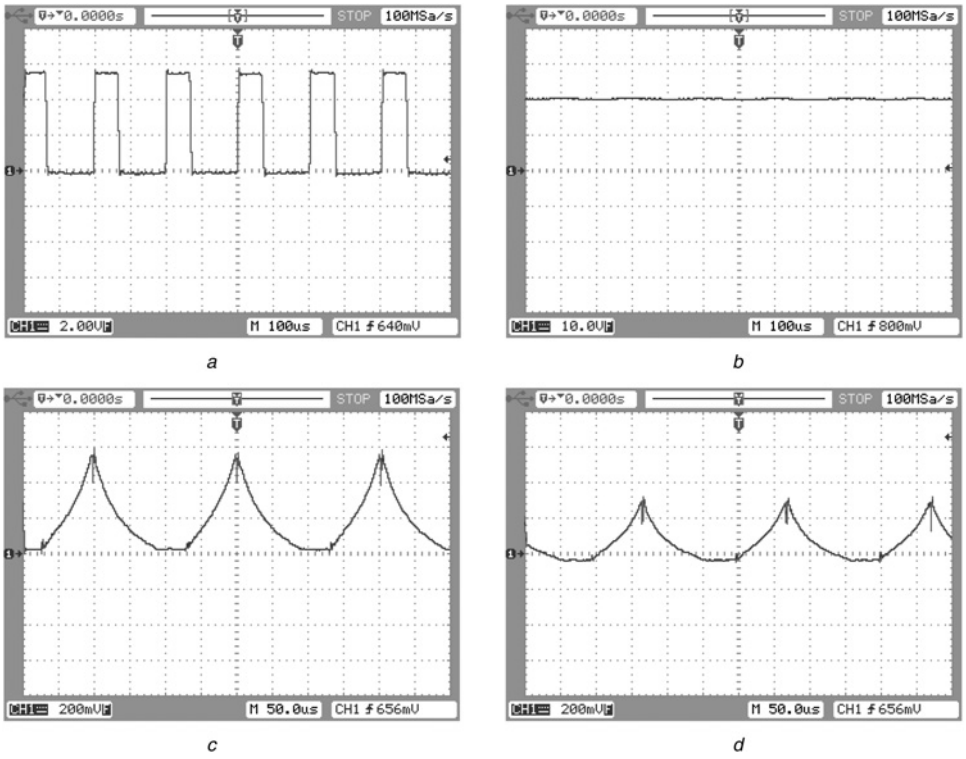

Fig. 10 *Typical waveforms in DCM*

a Duty cycle (D)

b Output voltage and its ripple

c Current of inductor L_1 $\left(i_{L_1}\right)$

d Current of inductor L_2 $\left(i_{L_2}\right)$

5 Conclusions

A novel DC/DC buck–boost converter is presented. The analysis of the presented converter is given in both the CCM and DCM operation modes. This converter has many advantages such as high voltage gain in comparison with conventional buck–boost and Cuk converters and broad CCM operation region. The presented converter has three operation modes in CCM. The second mode reduces the voltage stresses across the capacitors. Therefore the current stresses on diodes are also reduced. In this topology, only one power switch is used which decreases the switching power losses and the implementation cost of the presented converter. The experimental results are provided to verify the feasibility of the proposed converter.

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