A Switched-Capacitor DC–DC Converter With High Voltage Gain and Reduced Component Rating and Count

Wei Qian, Dong Cao, *Student Member, IEEE*, Jorge G. Cintrón-Rivera, *Student Member, IEEE*, Matthew Gebben, Dennis Wey, and Fang Zheng Peng, *Fellow, IEEE*

***Abstract*—This paper proposes a bidirectional switched-capacitor dc–dc converter for applications that require high voltage gain. Some of conventional switched-capacitor dc–dc converters have diverse voltage or current stresses for the switching devices in the circuit, not suitable for modular configuration or for high efficiency demand; some suffer from relatively high power loss or large device count for high voltage gain, even if the device voltage stress could be low. By contrast, the proposed dc–dc converter features low component (switching device and capacitor) power rating, small switching device count, and low output capacitance requirement. In addition to its low current stress, the combination of two short symmetric paths of charge pumps further lowers power loss. Therefore, a small and light converter with high voltage gain and high efficiency can be achieved. Simulation and experimental results of a 450-W prototype with a voltage conversion ratio of six validate the principle and features of this topology.**

***Index Terms*—Dc–dc power conversion, efficiency, modular, switched-capacitor, voltage gain.**

I. Introduction

SWITCHED-CAPACITOR DC–DC converters have gained popularity in industrial switched mode power supplies due to their attractive features such as magnetic-less structure and high efficiency. Since they can be easily integrated without bulky magnetic components, the power density of dc–dc converters can be significantly boosted. They can achieve high efficiency even at very light load condition and can maintain good no-load output voltage regulation [1]. Therefore, many switched-capacitor dc–dc converters [2]–[12] have been developed. Yet, conventional circuits that are usually used in low power applications have some of the following drawbacks when a high voltage gain is desired: 1) quite diverse voltage/current stresses for switching devices in some circuits, which are not suitable for modular configuration or for high efficiency requirement; 2) a large number of switching devices in some other circuits; 3) pulsating input current and the resultant electromagnetic interference (EMI); 4) unidirectional power flow. More importantly, their total device power ratings (TDPR) are unfavorable for a practical design to maintain high efficiency.

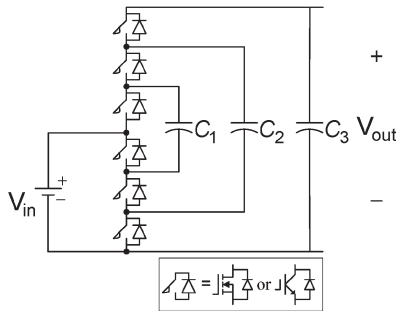

Fig. 1. Flying-capacitor dc–dc converter with the voltage conversion ratio of three.

To mitigate the pulsating current, voltage spike, and switching loss, resonant switched-capacitor converters have been proposed in [13]–[17] with additional inductor to resonate with the capacitor. Yet, their practical potential to reach high voltage gain has not been extensively investigated. Some combinations of switched-capacitor and inductors have been reported in [18]–[21] for large voltage conversion ratio, the easy integration and light weight feature of switched-capacitor dc–dc converters disappears after introducing relatively large inductors.

Recently, magnetic-less flying-capacitor (FC) dc–dc converters ([22]–[25]) and resonant FC dc–dc converters ([26], [27]) have been researched to virtually eliminate or to minimize the inductance requirement in traditional two-level dc–dc converters. Compared to low-power switched-capacitor converters, the magnetic-less FC dc–dc converters have the advantages of small component (switching device and capacitor) count, low voltage stress across the switching devices, and bidirectional power flow. One of such converters is shown in Fig. 1, with a conversion ratio of three (namely 3X). A 55-kW 3X dc–dc converter has been demonstrated as a promising candidate for

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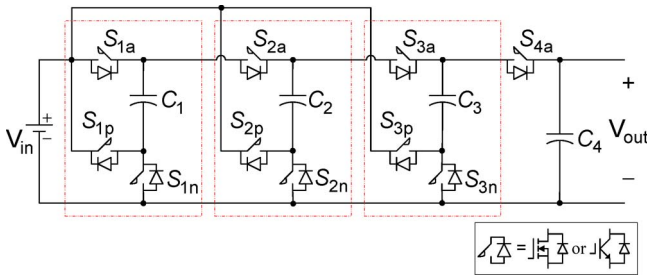

Fig. 2. Original MMCCC with a voltage conversion ratio of four.

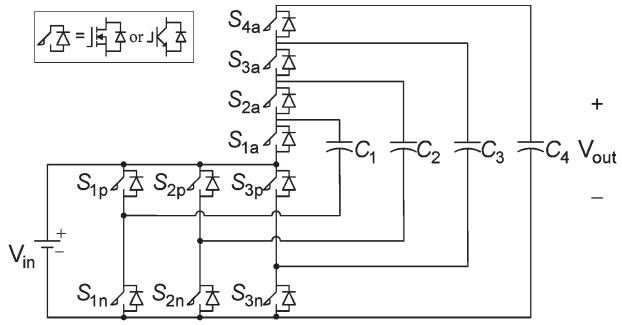

Fig. 3. MMCCC in the similar form as the flying-capacitor circuit.

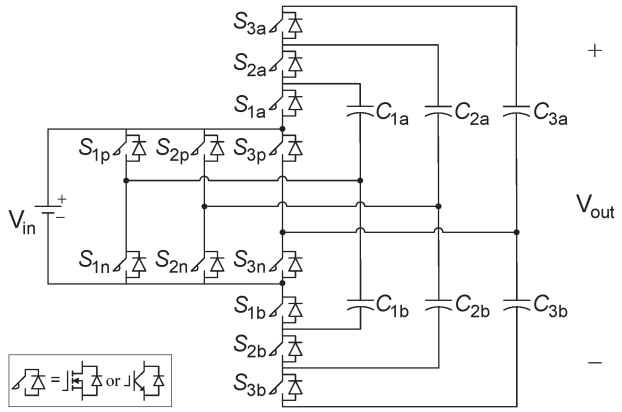

Fig. 4. Proposed 6X switched-capacitor dc–dc converter.

hybrid electric vehicles in [24], [25]. However, when it comes to high voltage conversion ratios, a pure magnetic-less FC structure has its practical limits to reach high voltage gain. For an output/input voltage boost ratio of N times (NX), the input current has to go through N switching devices. The resultant voltage drop and power loss overshadow their advantages presented at the low voltage ratios.

To address the above issues, a multilevel modular capacitor clamped dc–dc converter (MMCCC) was proposed in [28], [29]. A MMCCC is shown in Fig. 2, with a voltage conversion ratio of four. Improved efficiency can be expected, because: 1) the current to charge a capacitor flows through at most three switching devices, regardless of the voltage ratio; 2) the currents through the switching devices and capacitors reduce to roughly 2/N times the corresponding currents in the original FC structure for a voltage ratio of N, leading to the reduced TDPR. Recently, zero-current switching (ZCS) MMCCC [30] and its multiphase version [31] have been proposed, which employs distributed stray inductances present in each module to achieve zero current. It has good improvement, such as small resonant inductance requirement and no need for high capacitance. However, be hard switching or soft switching, the MMCCCs have 3N-2 switching devices, rather than 2N in the conventional FC structure. Moreover, the extra N-2 switching devices have to sustain the voltage stress of twice the input voltage (defined in boost mode). Additionally, as in many switched-capacitor dc–dc converters, while maintaining the device voltage (or current) stress low, it inevitably experiences the increased capacitor voltage with the increment of the voltage conversion ratio. The different voltage rating requirement and the maximum voltage rating of the capacitors pose challenges on component selection, size and efficiency, when a high voltage conversion ratio is desired.

This paper presents a switched-capacitor dc–dc converter that is very suitable for high voltage gain applications. It sums up the output of two symmetric charge pumps to reduce the device count, capacitor voltage rating, and power loss. Moreover, it keeps very low TDPR. As will be discussed later, its many merits lead to the possibility of a compact, light, and efficient converter. The following sections will start with a brief review on the structure of the MMCCC, such that the features of the proposed new converter could easily be brought to light. The operation principle and features of the proposed converter will be introduced afterward, followed by a quantitative comparison with other counterparts. The concept and analysis will be validated by simulation and experimental results.

II. Brief Review of the MMCCC Structure

The MMCCC as shown in Fig. 2 is composed of three basic cells, plus a switch S_{4a} and a capacitor C_4 connected to the output. In boost mode, it steps up the voltage from the low voltage input (defined as V_{in}) to the high voltage output (defined as V_{out}). From another point of view, the MMCCC can be reverted to the similar form as the FC circuit and can be redrawn in Fig. 3. The switch S_{ja} ($j = 1,\ 2,\ 3,\ 4$) creates a path for charging the capacitor C_j in one of two alternate switching states. The capacitor C_1 is charged by the input, V_{in}, and the other capacitor C_j ($j = 2,\ 3$) is charged via the addition of C_{j-1} and V_{in}. A phase leg of complementary switches S_{jp} and S_{jn} ($j = 1,\ 2,\ 3$) from each basic cell is in parallel with the input source V_{in}, in order that C_j can be directly connected to the positive (or negative) terminal of the input through just one switch S_{jp} (or S_{jn}). By the same token, the switching states are reduced from four to two, since the current path becomes independent. The above review explains why the MMCCC has shorter current paths and lower current stress than the FC converter as shown in Fig. 1 does.

III. Proposed Switched-Capacitor DC–DC Converter and Operation Principle

Fig. 4 shows the proposed switched-capacitor dc–dc converter with a voltage conversion ratio of six (named 6X). It can also function as a buck when the energy flows in the opposite direction. To explain the operating principle, its boost mode is taken as an example. The buck mode operation can be analyzed analogously. The charge pump splits into two

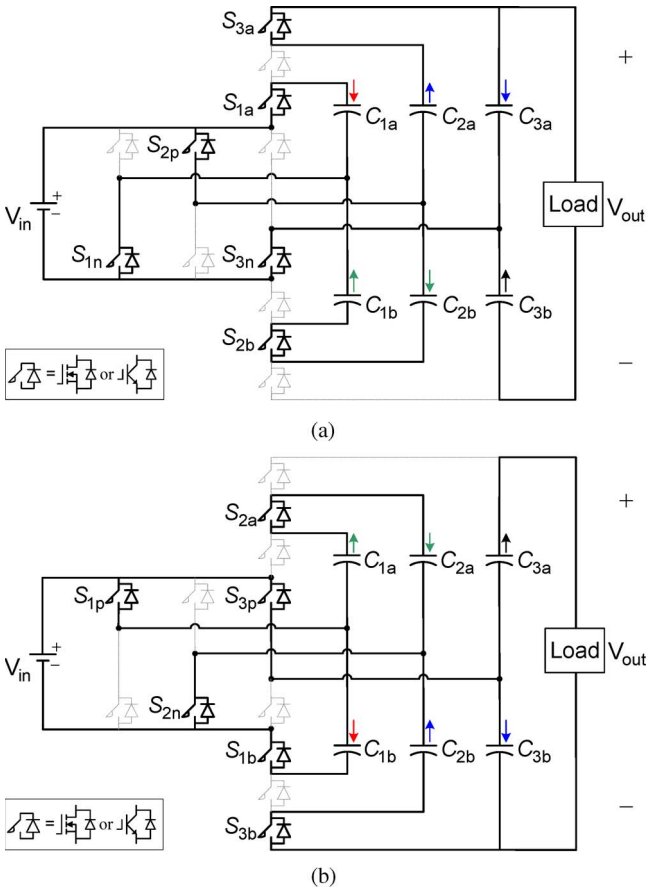

Fig. 5. Switching states of the 6X switched-capacitor dc–dc converter. (a) Switching states I. (b) Switching states II.

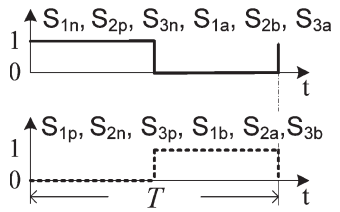

Fig. 6. Complementary PWM signals.

symmetric horizontal paths to build up the output voltage. In the upper path, the capacitor voltage is pumped up one by one to make the voltage of C_{3a} equal to $3V_{in}$; the lower path works in same manner, making the voltage of C_{3b} equal to $3V_{in}$.

This converter alternates between two switching states as shown in Fig. 5, with 50% duty ratio for each state as shown in Fig. 6. The switching devices marked in solid line are on-state devices and current paths; the remaining devices in dashed lines are off-state devices. Table I summarizes the switching states. The corresponding equivalent circuits are shown in Fig. 7. It is easy to infer that the switches S_{jp} and S_{jn} in the same phase leg are complementary; switches S_{ja} and S_{jb} are complementary as well (i.e., if one is on, the other should be off and vice versa. $j = 1,\ 2,\ 3$). In the switching state I as shown in Fig. 5(a), in the upper path, the capacitor C_{1a} is charged to V_{in} by the input through devices S_{1a} and S_{1n}, as simplified into an equivalent circuit in Fig. 7(a); the capacitor C_{2a} is in series with the input to charge the capacitor C_{3a} through the switches S_{2p},

TABLE I
CAPACITOR CHARGE PATHS IN TWO SWITCHING STATES

Switching state I		Switching state II	
Capacitor charge paths	On-state switches	Capacitor charge paths	On-state switches
$V_{in} \rightarrow C_{1a}\uparrow$	S_{1a}, S_{1n}	$V_{in} \rightarrow C_{1b}\uparrow$	S_{1b}, S_{1p}
$C_{2a}+V_{in} \rightarrow C_{3a}\uparrow$	S_{3a}, S_{3n}, S_{2p}	$C_{2b}+V_{in} \rightarrow C_{3b}\uparrow$	S_{3b}, S_{3p}, S_{2n}
$C_{1b}+V_{in} \rightarrow C_{2b}\uparrow$	S_{2b}, S_{2p}, S_{1n}	$C_{1a}\downarrow+V_{in} \rightarrow C_{2a}\uparrow$	S_{2a}, S_{2n}, S_{1p}

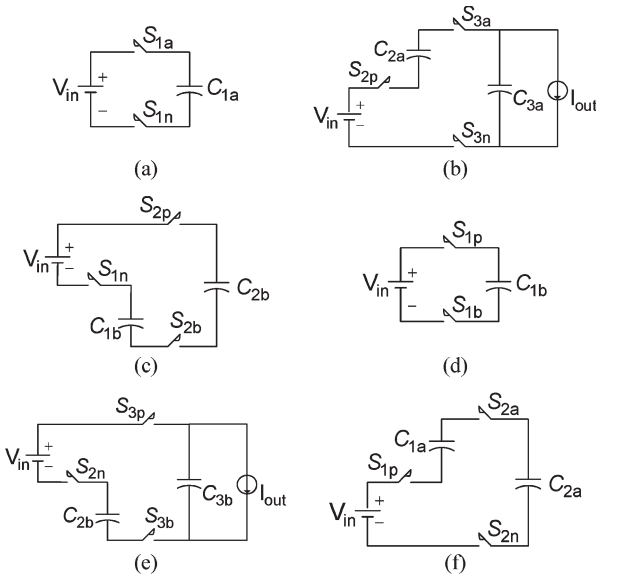

Fig. 7. Equivalent circuits for two switching states. (a) Charging C_{1a}. (b) Charging C_{3a}. (c) Charging C_{2b}. (d) Charging C_{1b}. (e) Charging C_{3b}. (f) Charging C_{2a}.

S_{3a} and S_{3n}, as simplified in Fig. 7(b). In the lower path, the capacitor C_{1b} is in series with the input to charge the capacitor C_{2b} through the switches S_{1n}, S_{2p} and S_{2b}, as simplified in Fig. 7(c). C_{3b} is discharged by the load current. In the similar way, in the switching state II as shown in Fig. 5(b), the complementary switches are gated on, so that the capacitors C_{2a}, C_{1b}, C_{3b} that are discharged in the first switching state become charged in the second switching state, while the capacitors C_{1a}, C_{3a}, C_{2b} become discharged. In particular, C_{3a} is discharged by the load current this time. Combining the voltage relations in the two switching states and neglecting the voltage drop, one can get the following voltage relations:

$$V_{Cja} = V_{Cjb} = j \times V_{in}, \quad j = 1, 2, 3. \tag{1}$$

Consequently, as the sum of the voltages across C_{3a} and C_{3b}, the output voltage is six times the input. In reality, the two capacitors, C_{ja} and C_{jb}, may be stabilized at a value slightly deviated from their theoretical values, because of the voltage drop, device tolerance, and possibly diverse gate delays as analyzed and addressed in [32]–[34]. Nevertheless, the possible voltage difference between a pair of capacitors, C_{ja} and C_{jb}, are tolerable during operation, since they are involved in two independent upper and lower charge paths, as can be seen from the equivalent circuits in Fig. 7.

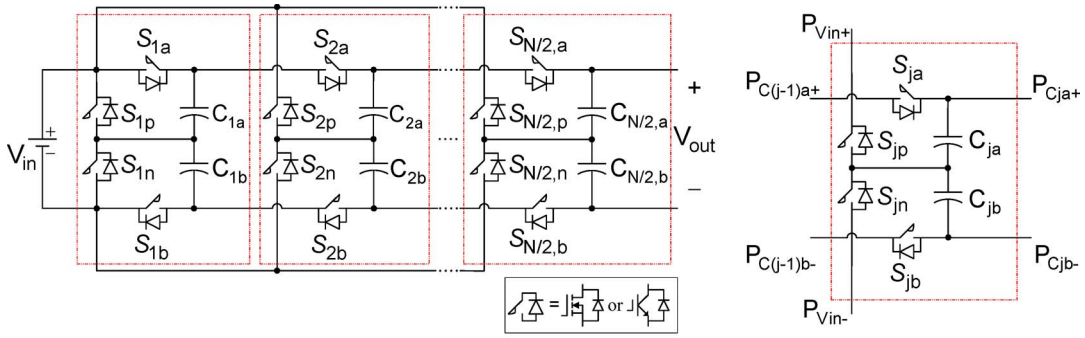

Fig. 8. Generalized NX switched-capacitor dc–dc converter constructed from basic modules. (a) The generalized NX switched-capacitor dc–dc converter. (b) Basic module.

IV. Characteristics of the Proposed Switched-Capacitor DC–DC Converter

Evidently, the new circuit shares some of the salient features as the MMCCC: short current paths and low current stress, which are preferable for high voltage gain and high efficiency. In addition, it is a modular structure as shown in Fig. 8(a). A generalized NX dc–dc converter consists of N/2 basic modules ($N = 2k,\ k = 1, 2, \ldots$) as shown in Fig. 8(b). Inside each module, a phase leg of two complementary switches $S_{\rm jp}$ and $S_{\rm jn} (j = 1, 2, 3, \ldots)$ and a pair of capacitors $C_{\rm ja}$ and $C_{\rm jb}$ are connected together at their respective midpoints. Externally, the switch phase leg is in parallel with the input voltage source; two terminals $P_{\rm Cja+}$ and $P_{\rm Cjb-}$ are connected to the next module; two terminals $P_{\rm C(j-1)a+}$ and $P_{\rm C(j-1)b-}$ from switches $S_{\rm ja}$ and $S_{\rm jb}$, respectively, are connected to the preceding module, except that the first module is directly fed by the input. Only the capacitor voltages in different modules differ, like in the MMCCC. Yet, in the new converter, since the capacitor voltages range from $V_{\rm in}$ to $N/2 \times V_{\rm in}$ in different modules, rather than from $V_{\rm in}$ to $NV_{\rm in}$ as in MMCCC, it is easier for a modular design. The modular structure can provide redundancy and fault tolerance [28]. A faulty module can be bypassed by redundant switching states, or be replaced by another module, such that the whole converter can continue operation.

Moreover, the new converter has its unique features, compared to the original MMCCC for the same NX voltage ratio:

1) Two charge pump paths feed the load directly, leading to less power loss in the energy transfer.
2) Half of the capacitors reduced their voltages by $N/2 \times V_{\rm in}$. Switched-capacitor dc–dc converters rely on capacitors to transfer energy and to filter the output voltage. Normally the larger equivalent series resistance (ESR) associated with the higher capacitor voltage rating lowers efficiency. Plus, capacitors contribute proportionally to the total volume and weight of the converter. High power density can be expected by employing low voltage capacitors.
3) There is lower capacitance and ripple current requirement for the two output capacitors. Given the same capacitance as in the MMCCC, the output voltage ripples are reduced in the new converter, because the two output capacitors are charged/discharged in an interleaved complementary way. It can be explained from the switching states in Fig. 5: while one of the capacitors is being charged, the other one is being discharged. Consequently, the sum of two complementary voltage ripples makes the output voltage almost ripple-free. This feature is quite beneficial if the converter operates at ZCS as the ZCS-MMCCC does in [30], such that the output voltage ripples can be minimized. Additionally, both output capacitors have smaller current ripples than the capacitors in the other basic modules, because they always supply load current while one of them gets charged alternatively.
4) The new converter employs fewer switches (2N versus 3N-2 in MMCCC) with no penalty of TDPR, as will be calculated in the later section. The associated gate drive and accessory power supply are saved accordingly. The number of switching devices, the floating gate drives and capacitors becomes large in switched-capacitor dc–dc converters for a high voltage gain. If unidirectional power flow is needed (e.g., in photovoltaic generation and thermoelectric generation), the MOSFETs $S_{\rm ja(b)}$ can be replaced by diodes. Thereby, only the switches $S_{\rm jp(n)}$ across the input dc bus remain, and a simpler bootstrap gate drive can be employed.
5) Each pair of complementary switching devices can be made truly capacitor-clamped. For instance, when $S_{2\rm a}$ in Fig. 8(a) is gated off, the voltage across $S_{2\rm a}$ is clamped by a natural clamp circuit formed by capacitors $C_{1\rm a}$, $C_{1\rm b}$, $C_{2\rm a}$, $C_{2\rm b}$ and the diode in $S_{2\rm b}$. This is a virtue for designing a high power converter without assistance from extra sunbber circuits.

In sum, its many features allow further higher efficiency with more compact package and lighter weight for high voltage boost gain than the MMCCC. Apparently, when N equals two, this converter reduces to the dc–dc converter module with a voltage conversion ratio of two in [35], in which very high efficiency was already demonstrated on a 10-kW converter.

Compared to the FC 3X dc–dc converter in [25], the proposed converter is more suitable for high voltage gain without voltage regulation. To accomplish regulation without compromising the high efficiency of the proposed converter, one approach is to add a second stage of dc–dc regulator. Since the second stage is dedicated only for regulation, high power density and high efficiency can still be expected from the two-stage power architecture, as reported in [22].

V. Component Cost Comparison With Other Topologies

To compare the cost of the new converter with its counterparts, the TDPR, the capacitor voltage stress, current rating, and capacitance requirement are itemized. TDPR is an indication of how much total silicon area is needed for the semiconductor devices. Here, it is based on the product of the maximum voltage imposed on the device and the average current flowing through it over the duration when the device conducts. Note that neither the peak current nor RMS current is used. In this way, the comparison is less dependent on the actual shape of the charge and discharge current, which is a function of the ESR and equivalent series inductance (ESL).

A. Total Device Power Rating

1) If the aforementioned 3X FC dc–dc converter (Fig. 1) is extended to an NX structure, all the 2N devices would have to sustain the voltage equal to the input voltage and the input current. Its TDPR is the same as the traditional boost converter

$$TDPR_{FC} = 2N \cdot (V_{\text{in}} \cdot I_{\text{in}}) = 2N \cdot P_{\text{in}} \tag{2}$$

where V_{in} is the input voltage and I_{in} is the input current.

2) The MMCCC also pumps charge from one capacitor to the next one, but its switching states reduce to two. Thus, the charge current into one capacitor is the discharge current from its preceding capacitor, except that the output capacitor has half the charge and discharge currents. Also, considering that the average charge current of one capacitor in half switching period equals its average discharge current in the other half switching period, the average current through each switching device is $2I_{out}$ in one of the two switching states. There are (N-2) switches sustain twice the input voltage, as stated earlier. Thus, the TDPR is

$$\begin{aligned}\text{TDPR}_{\text{MMCCC}} &= 2N \cdot V_{\text{in}} \cdot (2I_{out}) + (N-2) \cdot 2V_{\text{in}} \cdot (2I_{out}) \\ &= \frac{8N-8}{N} P_{\text{in}}, \qquad N = 2, 3, 4, \ldots .\end{aligned} \tag{3}$$

3) For the new converter, the (N-2) switches in the complementary phase leg convey the sum of the current in two charge pump paths, $4I_{out}$, which is twice the current through the rest switches. It is not hard to find the voltage stress of each switch. Hence, the TDPR can be derived as:

$$\begin{aligned}\text{TDPR}_{\text{new}} &= (N-2)V_{\text{in}} \cdot 4I_{out} + (2+2)V_{\text{in}} \cdot 2I_{out} \\ &\quad + (N-2)2V_{\text{in}} \cdot 2I_{out} \\ &= \frac{8N-8}{N} P_{\text{in}}, \qquad N = 2, 4, 6, \ldots .\end{aligned} \tag{4}$$

The above equations clearly demonstrate that unlike the conventional FC structure, the new converter has no penalty of TDPR even with fewer devices than the MMCCC. The ratio of the TDPR and the input power is plotted with respect to the voltage gain in Fig. 9. It is quite interesting that this ratio for the new converter will get saturated as N approaches infinite. This

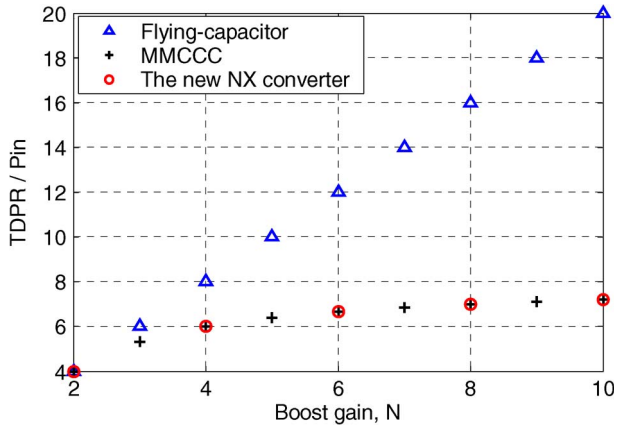

Fig. 9. Normalized total device power rating versus voltage boost gain.

property implies that the proposed converter requires less silicon area than the FC dc–dc converter does. It can be physically explained by the aforementioned fact that the charge/discharge current will only go through three switching devices at most, and that the maximum switching device voltage stress is no more than $2V_{\text{in}}$, in spite of voltage gain increment.

B. Capacitor Voltage, Current, and Capacitance Requirement

Table II compares the total capacitor voltage, the current, and the capacitance of the new converter with that of the FC and MMCCC. While the voltage ratings for the FC and the MMCCC are the same, the voltage rating for the new converter is reduced nearly by half, as plotted in Fig. 10. The RMS current is related to the parasitic parameters in the circuit, but the average charge (/discharge) current of the internal capacitors in the new converter (and in the MMCCC) can be calculated as 2/N times of the current in the FC dc–dc converter, as stated before; the average charge (/discharge) current of the two output capacitors is 1/(N-1) times of that in the FC dc–dc converter. Thereby, the capacitance requirement can be obtained accordingly. The quantitative comparison supports the earlier statement that the ripple current and capacitance requirement of the two output capacitors in new converter can be much lower.

VI. Practical Design Consideration

Switched-capacitor dc–dc converters used to be designed with sufficiently large capacitance to limit the peak charge current. Alternatively, they can be designed with much smaller capacitance by utilizing ESL present in the circuit [35]. Plus, the front edge of peak current is smoothed out thanks to ESL. The ESL requirement is discussed in this section.

A 450-W 6X dc–dc converter is implemented in three modules as shown in Fig. 11. Most ESL exists in the connection between two adjacent modules. However, it should be noted that ESL is minimized between the distributed input capacitors and the switches $S_{\text{jp(n)}}$ in every module. The switching frequency is 100 kHz. MOSFETs IRF1324S-7PPbF are employed for the devices $S_{\text{jp(n)}}$, and IRFS3004-7PPbF are for $S_{\text{ja(b)}}$. Based on Table II, 12, eight and six multilayer ceramic capacitors (MLCCs) C5750X7S2A106M are in parallel for $C_{\text{1a(b)}}$,

TABLE II
COMPARISON OF CAPACITOR VOLTAGE RATING, CURRENT, AND CAPACITANCE

	Total capacitor voltage ratings	Average charge/discharge current	Capacitance requirement
FC	$\frac{(1+N)N}{2}V_{in}$	$I_j=\begin{cases}N\cdot I_{out}, & (j=1,2,...,N-1)\\(N-1)\cdot I_{out}, & (j=N)\end{cases}$	$C_j=\begin{cases}\frac{I_{out}}{f_s\Delta V_j}, & (j=1,2,...,N-1)\\\frac{(N-1)I_{out}}{Nf_s\Delta V_j}, & (j=N)\end{cases}$
MMCCC	$\frac{(1+N)N}{2}V_{in}$	$I_j=\begin{cases}2I_{out}, & (j=1,2,...,N-1)\\I_{out}, & (j=N)\end{cases}$	$C_j=\begin{cases}\frac{I_{out}}{f_s\Delta V_j}, & (j=1,2,...,N-1)\\\frac{I_{out}/2}{f_s\Delta V_j}, & (j=N)\end{cases}$
New converter	$\frac{(1+N/2)N}{2}V_{in}$ $(N=2,4,6,...)$	$I_{ja}=I_{jb}$ $=\begin{cases}2I_{out}, & (j=1,2,...,\frac{N-1}{2})\\I_{out}, & (j=\frac{N}{2})\end{cases}$	$C_{ja}=C_{jb}$ $=\begin{cases}\frac{I_{out}}{f_s\Delta V_j} & (j=1,2,...,\frac{N-1}{2})\\\frac{I_{out}/2}{f_s\Delta V_j} & (j=\frac{N}{2})\end{cases}$

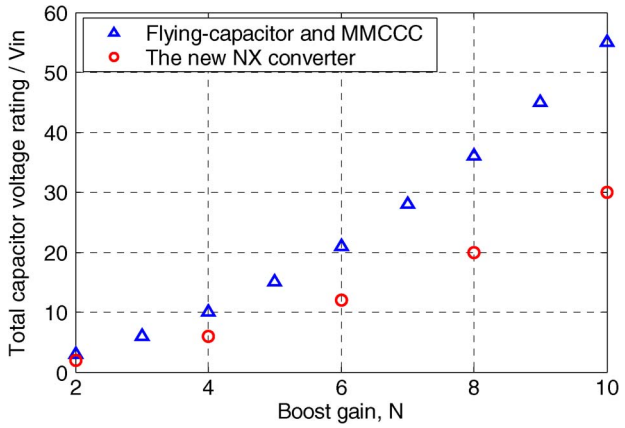

Fig. 10. Normalized total capacitor voltage rating versus voltage boost gain.

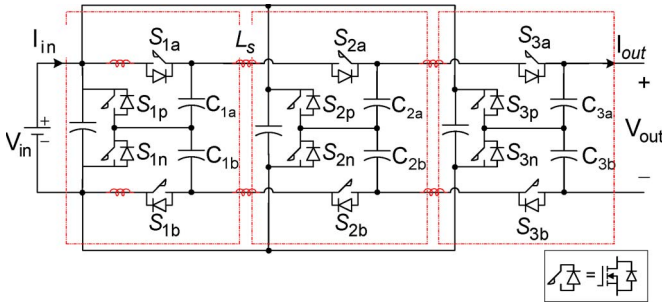

Fig. 11. Simulation and experimental configuration.

$C_{2a(b)}$, $C_{3a(b)}$, respectively. The effective capacitance at their corresponding voltages is: $C_{1a(b)}\approx 120\ \mu$F, $C_{2a(b)}\approx 60\ \mu$F, $C_{3a(b)}\approx 40\ \mu$F, according to the manufacture's data. There is only one capacitor in the charge loops as shown in Fig. 7(a) and (d), but two capacitors in the rest circuits. Thus, the equivalent loop capacitance is

$$C_{loopj}=\begin{cases}C_j, & j=1\\C_{j-1}\cdot C_j/(C_{j-1}+C_j), & j=2,3\end{cases} \quad (5)$$

where C_j is short for $C_{ja(b)}$.

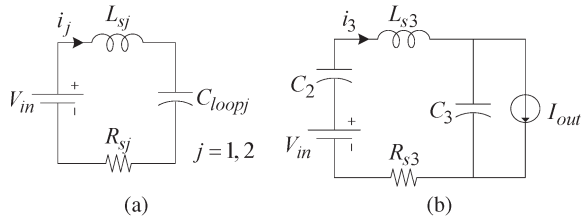

Fig. 12. Simplified equivalent circuits. (a) Internal charge loops. (b) Charge loop for the output capacitor.

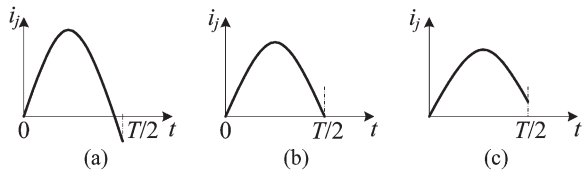

Fig. 13. Charge current with different resonant frequency f_r. (a) $f_r > f_s$. (b) $f_r = f_s$. (c) $f_r < f_s$.

The initial current in every charge loop starts from zero. For the internal charge loops as shown in Fig. 12(a), the charge current can be calculated as

$$i_j(t)=e^{-\alpha_j t}C_{loopj}\Delta V_{dj}\frac{\alpha_j^2+\omega_{dj}^2}{\omega_{dj}}\sin\omega_{dj}t$$
$$=e^{-\alpha_j t}\frac{I_{out}T}{2}\frac{\alpha_j^2+\omega_{dj}^2}{\omega_{dj}}\sin\omega_{dj}t,\quad for\ i=1,2 \quad (6)$$

where $\alpha_j=R_{sj}/(2L_{sj})$, $\omega_{dj}=\sqrt{1/(L_{sj}C_{loopj})-\alpha_j^2}$ for all the loops; T is the switching period. The initial voltage differences, $\Delta V_{d1}=(1/2)\cdot 2I_{out}\cdot(T/2)(1/C_1)$, $\Delta V_{d2}=(1/2)\cdot 2I_{out}\cdot T/2(1/C_1+1/C_2)$ are based on half of the capacitor voltage ripples.

The current is shown in Fig. 13 for three cases that the resonant frequency f_r is above, equal to and below a given switching frequency, f_s. For the same input power and voltage, their average current is the same. The current turns to negative in Fig. 13(a), which reduces the effectively transferred

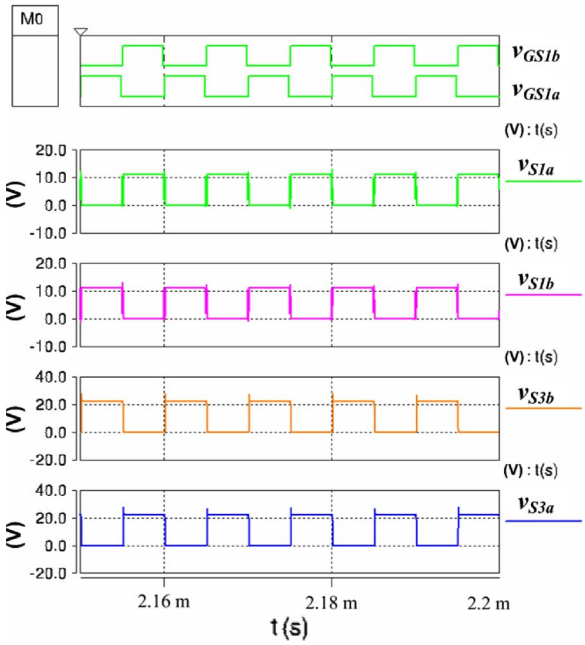

Fig. 14. Simulation results of gate drive signals and typical switch voltages.

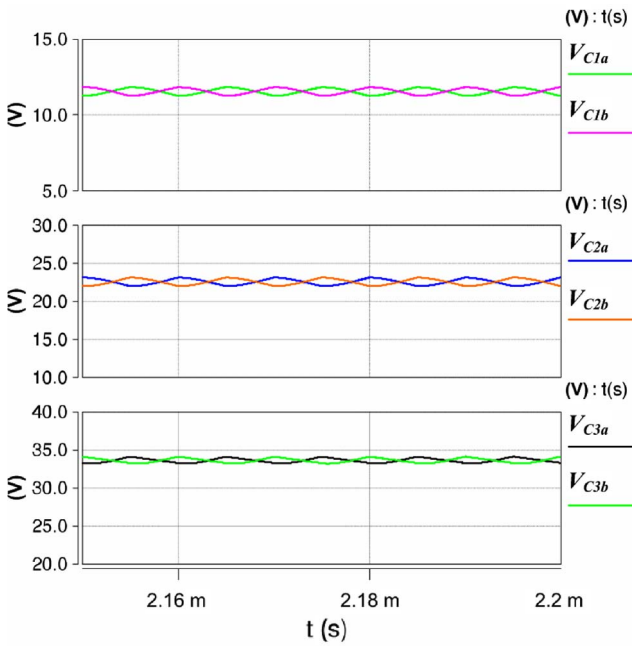

Fig. 15. Simulation results of capacitor voltages.

power and degrades efficiency. Hence, given fixed capacitance, minimum ESL needs to be designed according to the critical zero-current condition as shown in Fig. 13(b). Practically, the capacitance of MLCCs varies with the applied voltage, and is affected by tolerance particularly after aging. As a result, the resonant frequency of individual charge loops can vary. In the bidirectional converter that operates in two complementary switching states, exact ZCS may not be achieved in every MOSFET, even if the switching frequency is tuned up dynamically. Therefore, when the circuit has been designed, the operating switching frequency should be equal to or above the highest resonant frequency of all three modules.

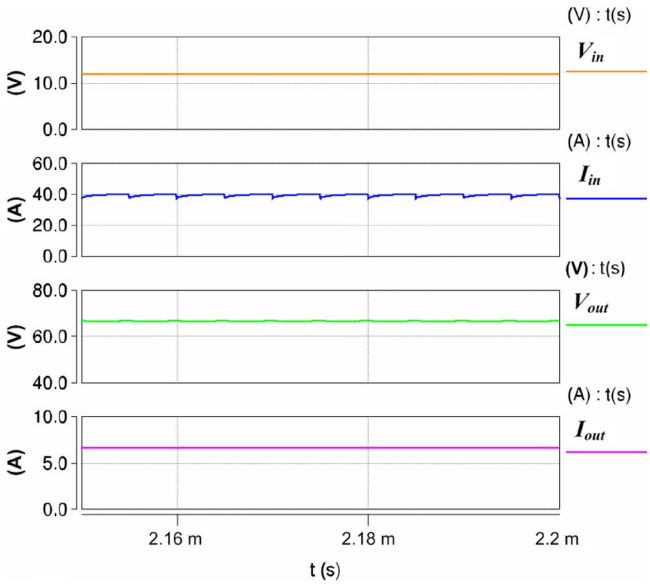

Fig. 16. Simulation results of input/output voltages and currents.

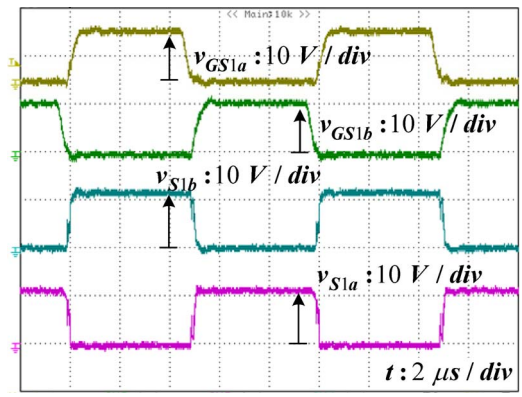

Fig. 17. Experimental results of complementary gate drive signals and the corresponding switches.

For the final charge loop whose equivalent circuit is shown in Fig. 12(b), the current charging the output capacitor is:

$$i_3(t) = \frac{C_2 I_{out}}{C_2 + C_3}\left[e^{-\alpha_3 t}(k_1 \cdot \sin\omega_{d3}t - \cos\omega_{d3}t) + 1\right] \quad (7)$$

where $k_1 = \{(\alpha_3^2+\omega_{d3}^2)[T/4(C_2+2C_3)/C_2 - C_2C_3R_{s3}/(C_2+C_3)] + \alpha_3\}/\omega_{d3}$.

From (7), it can be found that the minimum ESL for this stage is smaller than the ESL in its preceding stages for zero-current critical condition. Moreover, it is independent of output current. In sum, according to (6) and (7), if not considering ESR, the minimum ESL requirement is 21 nH, 63 nH, and 84 nH for the first, second, and third modules, respectively. The ESL is smaller when the switching frequency is higher. Conversely, a small air-core inductor can be added in case that the ESL is not sufficient.

VII. Simulation and Experimental Verification

The principle and analysis are verified by simulation and experiments of the 450-W prototype. Simulation results were

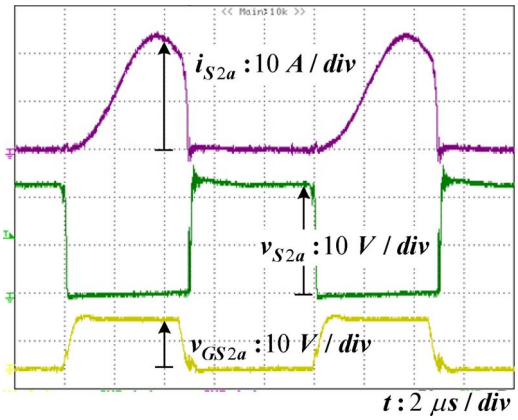

Fig. 18. Experimental results of the current, voltage and gate drive signal for switch V_{S2a}.

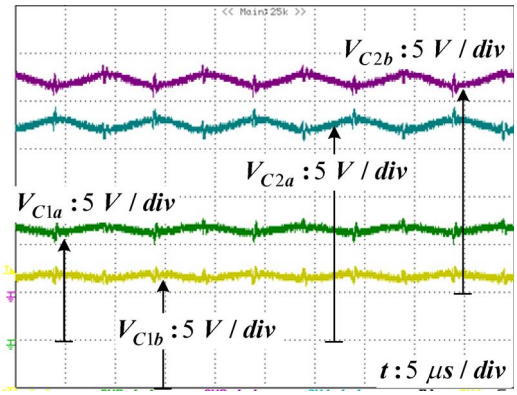

Fig. 19. Experimental results of capacitor voltage $V_{\mathrm{C1a(b)}}$ and $V_{\mathrm{C2a(b)}}$.

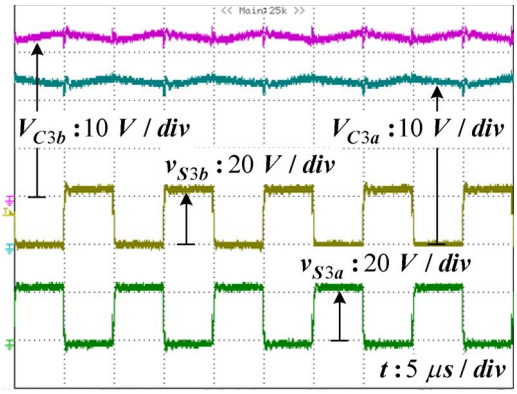

Fig. 20. Experimental results of capacitor voltage $V_{\mathrm{C3a(b)}}$ and switches $v_{\mathrm{S3a(b)}}$.

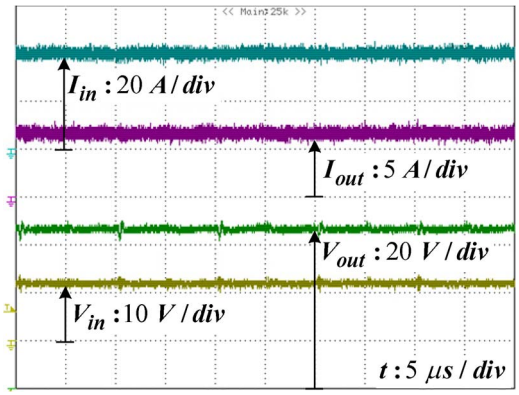

Fig. 21. Experimental results of input/output voltage and current.

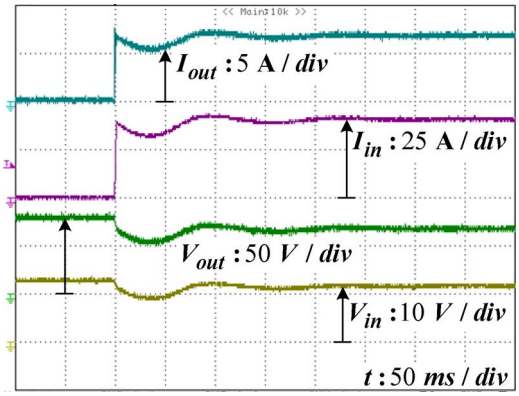

Fig. 22. Experimental results of load changes from open circuit to full load.

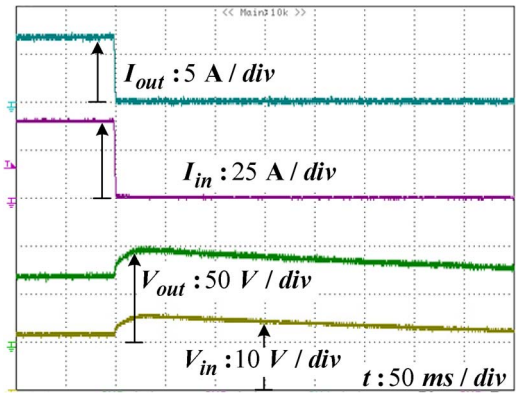

Fig. 23. Experimental results of load changes from full load to open circuit.

shown in Figs. 14–16. In Fig. 14, v_{GS1a} and v_{GS1b} represent two complementary gate drive signals, and voltages $v_{\mathrm{S1a}}(/v_{\mathrm{S1b}})$ and $v_{\mathrm{S3a}}(/v_{\mathrm{S3b}})$ represent two kinds of voltage stress across the switching devices. The capacitor voltages are shown in Fig. 15. The input/output voltages and currents are shown in Fig. 16. The experimental results are given in Figs. 17–23. The output voltage is boosted from a 12-V input to 68.2 V at 465-W output. Fig. 18 shows the typical voltage and current waveforms of one switch, $S_{2\mathrm{a}}$, captured at full power. Some voltage ringing is observed due to the inserted wire for measuring the current. However, no snubber circuit is used. Since the amplitude of the maximum voltage change is $2V_{\mathrm{in}}$, much less than a traditional converter's, EMI generated by dv/dt is limited [4]. As predicted, the ESL in the circuit smoothes the front edge of the charge current. The absence of current spike presents minimum EMI caused by di/dt [4], [8], [13]. In Figs. 19 and 20, two symmetric capacitors in one basic module have the same very low average voltage and nearly complementary voltage ripples. Hence, the output voltage ripple is quite small as shown in Fig. 21. The input current, I_{in} refers to the current before the capacitors across the input dc bus as shown in Fig. 11, due to the accessibility.

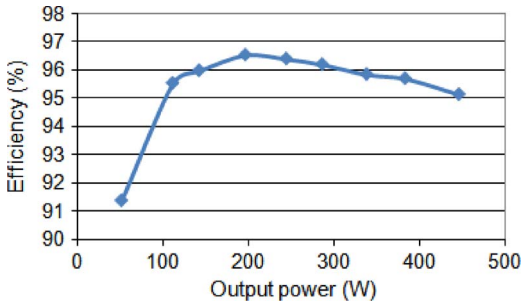

Fig. 24. Tested efficiency with respect to output power at 100-kHz switching frequency.

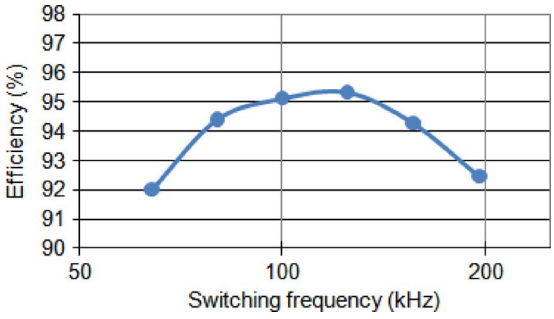

Fig. 25. Tested efficiency with respect to switching frequency at full load.

Figs. 22 and 23 show the dynamic response between the no load to full load.

Efficiency was measured with a Yokogawa WT1600 digital power meter. Fig. 24 shows the efficiency with respect to output power at 12-V input voltage and 100-kHz switching frequency. The measured 12-V gate drive power loss of 2.9 W was included. Fig. 25 is the measured efficiency at 450 W with different switching frequency, including gate drive losses. The optimal efficiency falls in the range from around 100 $\sim$ 125 kHz.

VIII. Conclusion

A novel switched-capacitor dc–dc converter with the potential of high voltage gain is proposed. Compared to its switched-capacitor dc–dc converter counterpart, it has the following advantages.

1) It has less power loss due to the two symmetric short paths of charge pumps;
2) It substantially reduces total capacitor voltage ratings;
3) It lowers capacitance and ripple current requirement of the output capacitors;
4) It has a reduced switching device count, low device current stress and low TDPR;
5) It improves efficiency and lowers cost;
6) It is able to have bidirectional operation;
7) It features a quasi modular structure that makes it very suitable for high-voltage gain applications.

Simulation and experimental results have verified the operation principle and features.

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