Abstract—This paper proposes the algorithm for selecting the parameters to improve the power factor in a PWM boost AC chopper topology. The phase angles of supply current, output current and output voltage are analyzed. The information of these phase angles is used to select the optimal capacitance value of capacitor filter. This process results the converter operating at unity input power factor. The simulation results by Pspice program are used to confirm the proposed technique.

Keywords: PWM boost AC chopper, capacitor filter, power factor

1. INTRODUCTION

Many applications, such as industrial heating, lighting control, soft start induction motors and speed controllers for fans and pumps require variable AC voltage from fixed AC source. The phase angle control of regulators has been widely used for these requirements. It offers some advantages such as simplicity and ability of controlling a large amount of power economically. However, delayed firing angle causes discontinuous and plentiful harmonics in load current and a lagging input power factor occurs at the AC side when the firing angle increased (M. H. Rashid 1993).

These problems can be solved by PWM AC chopper technique (B. W. Williams 1982; S. A. Bhat et al., 1982; G. H. Choe et al., 1989). In this technique, the input AC supply voltage will be controlled by PWM signal. This process produces the chopped output voltage that consists of fundamental and high-order harmonics. The high-order harmonic content of this voltage will be filtered out by low pass filter circuit. This results a sinusoidal output current and voltage. Although, the performance in case of input PF of PWM AC chopper is higher than the case of phase angle control technique, it depends on load power factor (B. H. Kwon et al., 1996; N. A. Ahmed et al., 1999; B. H. Kwon et al., 1999). This means the input PF will be low if the load power factor is low. The low input PF in the PWM AC chopper topologies was the concerned problem. To produce PWM signal for improving the input PF, the triangular carrier signal was modified (D. Jang et al., 1995). Some techniques used the cotangent curve (D. Jang et al., 1995) and the sinusoidal signal (K. Georgakas et al., 2009) to modify the DC reference signal. However, these techniques are difficult to implement and apply in the feed-back control. To improve the input PF without those modifications, therefore, this paper proposes the algorithm for selecting the optimal
capacitance value of capacitor filter to shift the phase angle of supply current close to the phase angle of supply voltage. The result of this process is that the converter can operate at unity input PF.

This paper is organized as the following sections. Section 2 presents a description of the PWM boost AC chopper topology and control circuit. In Section 3, the phase angles of supply current, output current and voltage are analyzed. Finally, in this section, we analyze the optimal capacitance value of $C_o$ and show the designed step finding the converter parameters for unity input PF. Section 4 shows the simulation results by Pspice program. In the last section, the conclusions are presented.

2. DESCRIPTION OF PWM BOOST AC CHOPPER

The power circuit of the PWM boost AC chopper is shown in Fig. 1 (a). This circuit consists of inductor $L$, capacitor filter $C_o$ and four power switches. The parallel-connected switches $s_{1-2}$ provide the energy in inductor $L$ when they are turned on by PWM control. The stored energy in inductor is transferred to the load through the series-connected switches $s_{3-4}$ while the switches $s_{1-2}$ are turned off. The switching patterns of controlled switches are decided by the polarity of the output voltage as shown in Fig. 1 (b). When the output voltage is positive, the switch $s_2$ and $s_4$ are fully turned on for feedback diode path and for transferring path. While the switch $s_1$ is turned on by duty cycle $D$ for storage mode and the switch $s_3$ is turned on by $1-D$ for suppressing the transient voltage at $v_p$ node. The switching patterns of all switches, when, the output voltage is negative, are opposite of when the output voltage is positive, respectively. Figure 1 (c) shows the logic circuit for actuating the controlled switches, which is simple to implement.

3. ANALYSIS

To find the optimal converter parameters, we firstly obtain an equivalent circuit for the PWM boost AC chopper. We assume that all components are ideal and the switching frequency $f_s$ is much greater than the supply frequency $f_i$.

3.1 Equivalent Circuit

During a switching period the supply and output voltage can be considered constant. In the average model of the switching converter, the average inductor voltage during one switching period is given by

$$v_L(t) = Dv_i(t) + (D-1)[v_o(t)-v_i(t)]$$  \hspace{1cm} (1)

where $v_i(t)$ and $v_o(t)$ are the average supply and output voltages during the switching period, respectively, and $D$ is the duty ratio. When the supply and output voltages are induced on the inductor by PWM switches in the high-frequency switching converter. They are slowly varying compared with the switching period $T_s$, it is possible to approximate the average inductor voltage as the following:

$$v_L(t) = L \frac{di_L(t)}{dt}$$  \hspace{1cm} (2)

where $i_L(t)$ is the average inductor current during the switching period. The inductor current produces the output current $i_o(t)$ during the discharging mode while the inductor current is caused by the supply current. Hence, the following relations are obtained:
where \( i_o(t) \) and \( i_L(t) \) are the average output and supply currents, respectively, during the switching period. From equations (1) and (2), the following relation is obtained:

\[
Dv_i(t) = L\frac{d}{dt}i_L(t) + (1-D)[v_o(t) - v_i(t)]
\]

(5)

Furthermore, equation (5) gives rise to

\[
v_i(t) = \frac{L}{1-D} \frac{d}{dt}i_o(t) + v_o(t)
\]

(6)

Equation (6) represents an equivalent circuit for the PWM boost AC chopper shown in Fig. 2.

3.3 Optimal Capacitance for Unity Power Factor

To obtain the capacitance of \( C_o \) producing unity power factor at input side, we assume that there is no the capacitor filter \( C_o \) in the equivalent circuit in Fig. 2. Therefore, the transfer function of the output voltage \( V_o(s) \) with respect to the supply voltage \( V_i(s) \) is obtained as

\[
\frac{V_o(s)}{V_i(s)} = \frac{sL_o(1-D) + R_o}{sL_o(1-D)^2 + L_o(1-D) + R_o(1-D)^2}
\]

(7)

From (7), we get the phase angle between \( V_o(s) \) and \( V_i(s) \) as following:

\[
\theta_{vo} = \tan^{-1}\theta_v - \tan^{-1}\theta_i = \tan^{-1}\left(\frac{L_o(1-D)}{R_o(1-D)^2 + L_o(1-D)}\right)
\]

(8)

3.2 Effect of Capacitance value of \( C_o \)

In the equivalent circuit Fig. 2, the main function of capacitor \( C_o \) is to filter out the high-order harmonic content producing the sinusoidal output. The capacitance value of \( C_o \) affect output voltage ripple (M. H. Rashid 1993). Moreover, it affects the input PF. To explain its effect, we assume the equivalent circuit without the capacitor filter \( C_o \). Therefore, the output current, \( i_o \), is equal to the load current, \( i_{load} \). This means both currents have the same phase angle. Notice that the phase angle of \( i_o \) is equal to the phase angle of inductor and supply currents. This causes the input PF \( \cos \theta_i \) depending on load power factor. This assumption is shown in Fig. 3. When the capacitor \( C_o \) is inserted into the circuit, the phase angle of supply current, \( \theta_i \), will be closely shifted to the phase angle of supply voltage, \( \theta_i \). Therefore, we can find the optimal capacitance value of \( C_o \) for unity input PF.
\[ \theta_{\text{eq}} = -\tan^{-1}\omega \left( \frac{L_o(1-D)^2 + L}{R_o(1-D)^2} \right) \]  

Equations (8) to (10) show the phase angles of output voltage and inductor current which respect to the phase of supply voltage. These show that the input \( PF \) (\( \cos \theta_{eq} = \cos \theta_{\text{eq}} \)) depends on the inductor \( L \), duty cycle \( D \) and load impedance \( Z_L = R_o + j\omega L_o \). In some applications, the converter operates at the fixed duty cycle and load impedance. Therefore, we can design the converter parameters operating at unity power factor. Our objective is to obtain the capacitance value of \( C_o \) to make \( \theta_{eq} \) in phase with \( \theta_{vi} \). Considering Fig. 4, after the capacitor filter \( C_o \) is parallel connected with the output load, the phase angle of \( V_o \) is shifted to the phase angle of \( V_o \) by \( I_{L} \) and then is shifted to the phase angle of \( V_o \) by \( I_{L} \). This gives the \( \theta_{eq} \) in phase with \( \theta_{vi} \) resulting unity input power factor. Therefore, the capacitance value of \( C_o \) for improving the input power factor is obtained as the following:

\[ C_o = C_o' + C_o'' \]

\[ C_o = \frac{P \tan \theta_{\text{load}}}{\omega V_{\text{rms}}} + \frac{P \tan \theta_{\text{ani}}}{\omega V_{\text{rms}}} \]  

where

- \( C_o' \) is the capacitor for producing the current \( I_{C} \);
- \( C_o'' \) is the capacitor for producing the current \( I_{C} \);
- \( P \) is the real power of load;
- \( V_{\text{rms}} \) is the root mean square of output voltage.

3.4 Designing Example

This sub session show the guideline for designing the converter parameters. The assumption is that the converter system has input voltage 110 V, frequency 50 Hz, and an induction motor load requires 220 V, frequency 50 Hz to absorb power 1 kW at a lagging power factor 0.8. From this information, we design the converter parameters having the step as follows:

1. Finding the duty cycle;

\[ D = \frac{1 - 110}{220} = 0.5 \]

2. Finding the load impedance;

\[ R_o = \frac{V_{\text{rms}}^2 (\cos \theta_{\text{load}})^2}{P} = 31 \text{ \text{\Omega}} \]

and

\[ L_o = \frac{R_o \tan \theta_{\text{load}}}{2\pi \times 50} = 73 \text{ \text{mH}} \]

where \( \theta_{\text{load}} = \cos^{-1} 0.8 = 36.8^\circ \)

3. Finding the inductance value of \( L \): the converter operates at 25 kHz and requires the inductor current ripple \( \Delta i_L < 1 \text{V} \)

\[ L = \frac{V_i \times D \times T_s}{\Delta i_L} = \frac{155 \times 0.5 \times 0.04 \times 10^{-3}}{1} = 3.1 \text{ \text{mH}} \]

4. Finding the phase angle of output voltage using (8);

\[ \theta_m = 4^\circ \]

5. Using (11) to calculate \( C_o \)

\[ C_o = \frac{54\ \mu\text{F}}{} \]

4. SIMULATION RESULTS

This session shows the simulation results to confirm the proposed technique. The converter parameters as shown in the designed step 1 – 5 are simulated using Pspice program. The simulation results are illustrated in Fig. 5 - 8. Figure 5 (a) shows the load current and output voltage while Fig. 5 (b) shows the supply current and voltage. Although, load power factor is low at 0.8 lagging, the power factor at input side is unity. This is because of the optimal capacitance value of \( C_o = 54 \mu\text{F} \). Figure 6 (a) shows the variation of \( C_o \) affecting with input \( PF \). When \( C_o \) is reduced or increased from the optimal capacitance value, this causes lagging or leading input \( PF \), respectively. While Fig. 6 (b) shows the variation of duty cycle \( D \) versus input \( PF \). At low \( D \), the input \( PF \) is nearly unity, while at high \( D \), the input \( PF \) is low. This is because of the effect of changing in phase angle of inductor current, \( \theta_{L} \). However, this effect can be avoided by selecting the new capacitance value of \( C_o \) for the unity input \( PF \) at any \( D \) by using designed step 1 – 5.

In some cases of load impedance, the high ripple output voltage will be appeared at the output side because of small capacitance of \( C_o \). For an example in this case, assuming that the load impedance is \( Z_L = 50 \text{\Omega} \). Using the designed step 1 – 5, the optimal capacitance value is \( C_o = 5 \mu\text{F} \). The simulation results are shown in Fig. 7 (a) causing high ripple output voltage although the input \( PF \) is unity as shown in Fig. 7 (b). To reduce the ripple output voltage, \( C_o \) should be increased. However, this causes a reduction in input \( PF \) as shown in Fig. 8. Therefore, in converter designing the designer should consider this effect, and also select \( C_o \) for the optimal ripple output voltage and input \( PF \).
Fig. 5 Simulation results ($Z_L = 31 + j22.9\Omega$, $C_o = 54\mu F$, $L = 3.1\, mH$, $D = 0.5$, and $f_i = 25\, kHz$) (a) Output voltage and current; (b) Supply voltage and current.

Fig. 6 Variation of input power factor ($Z_L = 31 + j22.9\Omega$, $L = 3.1\, mH$ and $f_i = 25\, kHz$) (a) as a function of $C_o$, and (b) as a function of $D$.

Fig. 7 Simulation results ($Z_L = 50\Omega$, $C_o = 5\mu F$, $L = 3.1\, mH$, $D = 0.5$, and $f_i = 25\, kHz$) (a) Output voltage and current; (b) Supply voltage and current.

Fig. 8 Variation of input power factor ($Z_L = 50\Omega$, $L = 3.1\, mH$, and $f_i = 25\, kHz$) (a) as a function of $C_o$, and (b) as a function of $D$. 
5. CONCLUSION

In this paper, we indicate that the capacitance value of $C_o$ in PWM boost AC chopper topology affects the input power factor. To find the optimal capacitance value of $C_o$ for AC chopper operation, therefore, we analyze the phase angles of supply current, output current and voltage. The simulation results show that the AC chopper can operate at the unity input power factor.

REFERENCES


ACKNOWLEDGMENT

The authors would like to thank Faculty of Engineering, Mahasarakham University, Mahasarakham, Thailand, for the financial supporting of this project under grant of modern researcher development.

AUTHORS PROFILE

Apinan Aurasopon was born in Amnat-charoen Thailand in 1971. He received the B.Eng in Electronic Engineering from Northeastern colleague in 1995, M.Eng. and Ph.D. in Electrical Engineering from King Mongkut’s University of Technology Thonburi in 2003 and 2007, respectively. He was a lecturer at Department of Electrical Engineering, Faculty of Engineering, Burapha University (BU), Chonburi in 2007 and transferred to Faculty of Engineering, Mahasarakham University (MSU) in 2008 until now. His research interests including soft-switched converters, ac choppers, converter systems for improving power quality, and designing power converter for reactor-hydrogen.

Nawarat Piladaeng graduated from Konh Kaen University in 2006, M.E from University of Adelaide, South Australia, Australia in 2008. She is a lecturer at Department of Electrical Engineering, Faculty of Engineering, Mahasarakham University (MSU) in 2008 until now. Her research interests include image processing and circuit design.