Unity Input Power Factor for a PWM boost AC Chopper

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Abstract—This paper proposes the algorithm for selecting the parameters to improve the power factor in a PWM boost AC chopper topology. The phase angles of supply current, output current and output voltage are analyzed. The information of these phase angles is used to select the optimal capacitance value of capacitor filter. This process results the converter operating at unity input power factor. The simulation results by Pspice program are used to confirm the proposed technique.

Keywords: PWM boost AC chopper, capacitor filter, power factor

NOMENCLATURE

PWM	Pulse-width modulation
PF	Power factor
C_o	Capacitor filter
D	Duty cycle
L	Inductor
Z_L	Load impedance
$\mathbf{V}_i$	Phasor diagram of supply voltage
$\mathbf{V}_o$	Phasor diagram of output voltage
$\mathbf{I}_{Co}$	Phasor diagram of capacitor filter current
$\mathbf{I}_i$	Phasor diagram of supply current
$\mathbf{I}_L$	Phasor diagram of inductor current
f_i	Supply frequency
f_s	Switching frequency
i_i	Supply current
i_o	Output current
i_{load}	Load current
i_L	Inductor current
v_p	Chopped output voltage
v_i	Supply voltage
v_o	Output voltage
ω_i	Angular frequency of supply voltage (rad/s)
θ_{iload}	Phase angle of load current
θ_{i_i}	Phase angle of supply current
θ_{i_o}	Phase angle of output current
θ_{iL}	Phase angle of inductor current
θ_{vi}	Phase angle of supply voltage
θ_{vo}	Phase angle of output voltage

1. INTRODUCTION

Many applications, such as industrial heating, lighting control, soft start induction motors and speed controllers for fans and pumps require variable AC voltage from fixed AC source. The phase angle control of regulators has been widely used for these requirements. It offers some advantages such as simplicity and ability of controlling a large amount of power economically. However, delayed firing angle causes discontinuous and plentiful harmonics in load current and a lagging input power factor occurs at the AC side when the firing angle increased (M. H. Rashid 1993).

These problems can be solved by PWM AC chopper technique (B. W. Williams 1982; S. A. Bhat et al., 1982; G. H. Choe et al., 1989). In this technique, the input AC supply voltage will be controlled by PWM signal. This process produces the chopped output voltage that consists of fundamental and high-order harmonics. The high-order harmonic content of this voltage will be filtered out by low pass filter circuit. This results a sinusoidal output current and voltage. Although, the performance in case of input *PF* of PWM AC chopper is higher than the case of phase angle control technique, it depends on load power factor (B. H. Kwon et al., 1996; N. A. Ahmed et al., 1999; B. H. Kwon et al., 1999). This means the input *PF* will be low if the load power factor is low. The low input *PF* in the PWM AC chopper topologies was the concerned problem. To produce PWM signal for improving the input *PF*, the triangular carrier signal was modified (D. Jang et al., 1995). Some techniques used the cotangent curve (D. Jang et al., 1995) and the sinusoidal signal (K. Georgakas et al., 2009) to modify the DC reference signal. However, these techniques are difficult to implement and apply in the feed-back control. To improve the input *PF* without those modifications, therefore, this paper proposes the algorithm for selecting the optimal

capacitance value of capacitor filter to shift the phase angle of supply current close to the phase angle of supply voltage. The result of this process is that the converter can operate at unity input *PF*.

This paper is organized as the following sections. Section 2 presents a description of the PWM boost AC chopper topology and control circuit. In Section 3, the phase angles of supply current, output current and voltage are analyzed. Finally, in this section, we analyze the optimal capacitance value of C_o and show the designed step finding the converter parameters for unity input *PF*. Section 4 shows the simulation results by Pspice program. In the last section, the conclusions are presented.

2. DESCRIPTION OF PWM BOOST AC CHOPPER

The power circuit of the PWM boost AC chopper is shown in Fig. 1 (a). This circuit consists of inductor *L*, capacitor filter C_o and four power switches. The parallel-connected switches s_{1-2} provide the energy in inductor *L* when they are turned on by PWM control. The stored energy in inductor is transferred to the load though the series-connected switches s_{3-4} while the switches s_{1-2} are turned off. The switching patterns of controlled switches are decided by the polarity of the output voltage as shown in Fig. 1 (b). When the output voltage is positive, the switch s_2 and s_4 are fully turned on for feed back diode path and for transferring path. While the switch s_1 is turned on by duty cycle *D* for storage mode and the switch s_3 is turned on by 1-*D* for suppressing the transient voltage at v_p node. The switching patterns of all switches, when, the output voltage is negative, are opposite of when the output voltage is positive, respectively. Figure 1 (c) shows the logic circuit for actuating the controlled switches, which is simple to implement.

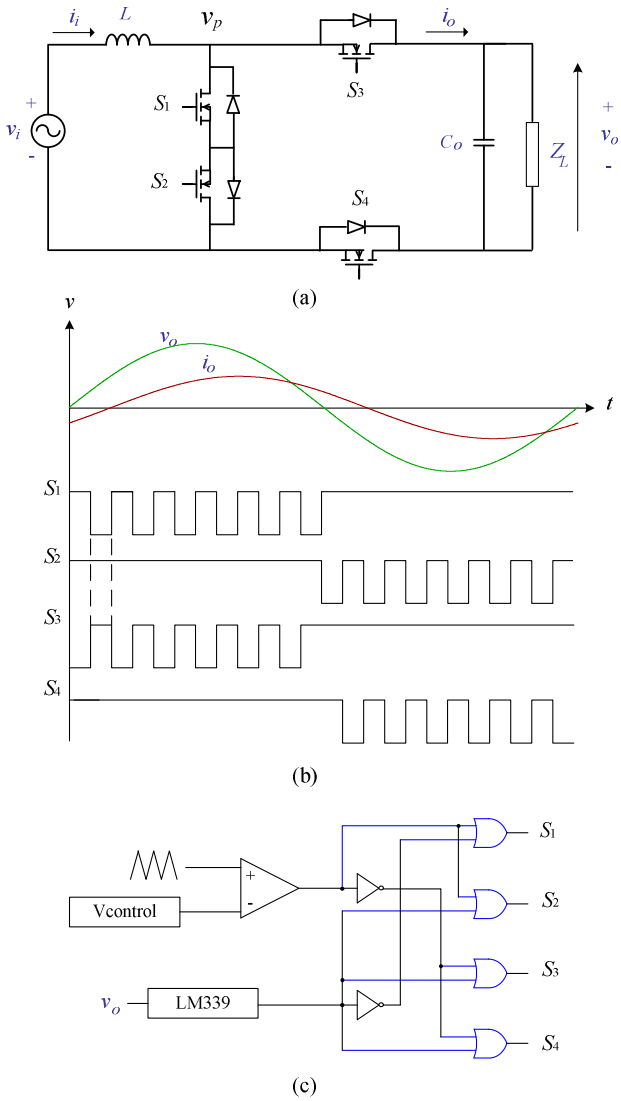

Fig. 1 Proposed PWM boost AC chopper voltage controller.
(a) Circuit configuration. (b) Switching pattern of gating signals.
(c) Block diagram of the control circuit.

3. ANALYSIS

To find the optimal converter parameters, we firstly obtain an equivalent circuit for the PWM boost AC chopper. We assume that all components are ideal and the switching frequency f_s is much greater than the supply frequency f_i.

3.1 Equivalent Circuit

During a switching period the supply and output voltage can be considered constant. In the average model of the switching converter, the average inductor voltage during one switching period is given by

$$v_L(t) = Dv_i(t) + (D-1)\left[v_o(t) - v_i(t)\right] \tag{1}$$

where $v_i(t)$ and $v_o(t)$ are the average supply and output voltages during the switching period, respectively, and *D* is the duty ratio. When the supply and output voltages are induced on the inductor by PWM switches in the high-frequency switching converter. They are slowly varying compared with the switching period T_s, it is possible to approximate the average inductor voltage as the following:

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{2}$$

where $i_L(t)$ is the average inductor current during the switching period. The inductor current produces the output current $i_o(t)$ during the discharging mode while the inductor current is caused by the supply current. Hence, the following relations are obtained:

$$i_o(t) = (1-D)i_L(t) \quad (3)$$

$$i_i(t) = i_L(t) \quad (4)$$

where $i_o(t)$ and $i_i(t)$ are the average output and supply currents, respectively, during the switching period. From equations (1) and (2), the following relation is obtained:

$$Dv_i(t) = L\frac{d}{dt}i_L(t) + (1-D)\left[v_o(t) - v_i(t)\right] \quad (5)$$

Furthermore, equation (5) gives rise to

$$\frac{v_i(t)}{1-D} = \frac{L}{(1-D)^2}\frac{d}{dt}i_o(t) + v_o(t) \quad (6)$$

Equation (6) represents an equivalent circuit for the PWM boost AC chopper shown in Fig. 2.

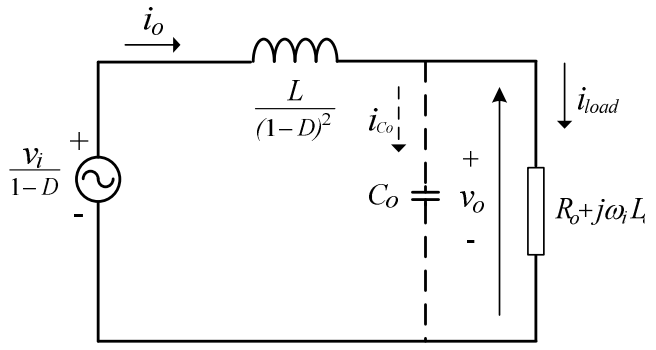

Fig. 2 Equivalent circuit for a PWM boost AC chopper.

3.2 Effect of Capacitance value of C_o

In the equivalent circuit Fig. 2, the main function of capacitor C_o is to filter out the high-order harmonic content producing the sinusoidal output. The capacitance value of C_o affect output voltage ripple (M. H. Rashid 1993). Moreover, it affects the input *PF*. To explain its effect, we assume the equivalent circuit without the capacitor filter C_o. Therefore, the output current, i_o is equal to the load current, i_{load}. This means both currents have the same phase angle. Notice that the phase angle of i_o, θ_{i_o}, is equal to the phase angle of inductor and supply currents. This causes the input *PF* ($\cos\theta_{i_i}$) depending on load power factor. This assumption is shown in Fig. 3. When the capacitor C_o is inserted into the circuit, the phase angle of supply current, θ_{i_i}, will be closely shifted to the phase angle of supply voltage, θ_{vi}. The phase θ_{i_i} will lead or lag the phase θ_{vi} depending on the capacitance value of C_o. Therefore, we can find the optimal capacitance value of C_o for unity input *PF*.

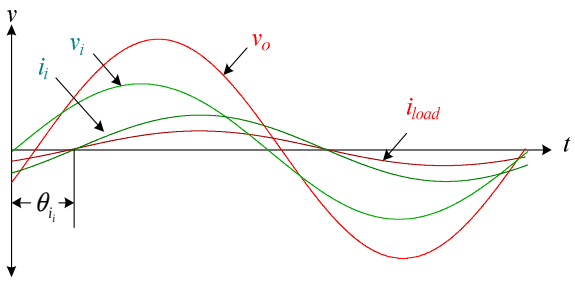

Fig. 3 Phase angles of current and voltage of equivalent circuit in Fig. 2 for the case of without C_o.

3.3 Optimal Capacitance for Unity Power Factor

To obtain the capacitance of C_o producing unity power factor at input side, we assume that there is no the capacitor filter C_o in the equivalent circuit in Fig. 2. Therefore, the transfer function of the output voltage $\mathbf{V}_O(s)$ with respect to the supply voltage $\mathbf{V}_i(s)$ is obtained as

$$\frac{\mathbf{V}_o(s)}{\mathbf{V}_i(s)} = \frac{sL_o(1-D) + R_o}{s\left[L_O(1-D)^2 + L\right] + R_O(1-D)^2} \quad (7)$$

From (7), we get the phase angle between $\mathbf{V}_O(s)$ and $\mathbf{V}_i(s)$ as following:

$$\theta_{vo} = \tan^{-1}\omega\left(\frac{L_o}{R_o}\right) - \tan^{-1}\omega\left(\frac{L_o(1-D)^2 + L}{R_o(1-D)^2}\right) \quad (8)$$

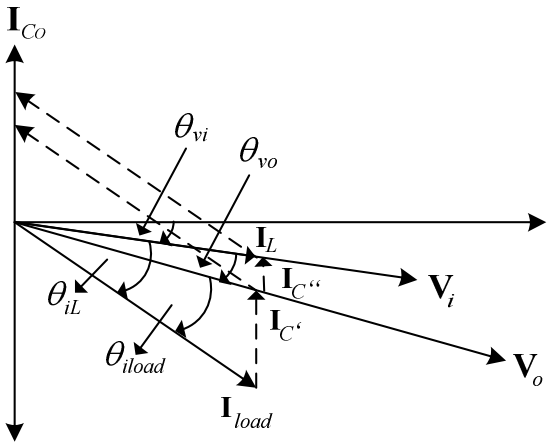

Fig. 4 Phasor diagram showing the effect of adding two capacitors in parallel with the inductive load.

From (3) and (7), the inductor current $\mathbf{I}_L(s)$ is given as:

$$\frac{\mathbf{I}_L(s)}{\mathbf{V}_i(s)} = \frac{1-D}{s\left[L_O(1-D)^2 + L\right] + R_O(1-D)^2} \quad (9)$$

Therefore, the phase angle between $\mathbf{I}_L(s)$ and $\mathbf{V}_i(s)$ is obtained as

$$\theta_{iL} = -\tan^{-1}\omega_i\left(\frac{L_o(1-D)^2+L}{R_o(1-D)^2}\right) \quad (10)$$

Equations (8) to (10) show the phase angles of output voltage and inductor current which respect to the phase of supply voltage. These show that the input *PF* ($\cos\theta_{iL} = \cos\theta_{i_i}$) depends on the inductor *L*, duty cycle *D* and load impedance $Z_L = R_o + j\omega_i L_o$. In some applications, the converter operates at the fixed duty cycle and load impedance. Therefore, we can design the converter parameters operating at unity power factor. Our objective is to obtain the capacitance value of C_o to make θ_{iL} in phase with θ_{vi}. Considering Fig. 4, after the capacitor filter C_o is parallel connected with the output load, the phase angle of $\mathbf{I}_L$ is shifted to the phase angle of $\mathbf{V}_o$ by $\mathbf{I}_{c'}$ and then is shifted to the phase angle of $\mathbf{V}_i$ by $\mathbf{I}_{c''}$. This gives the θ_{iL} in phase with θ_{vi} resulting unity input power factor. Therefore, the capacitance value of C_o for improving the input power factor is obtained as the following:

$$C_o = C_o^{'} + C_o^{''}$$

$$C_o = \frac{P\tan\theta_{iload}}{\omega_i \mathrm{V}_{orms}^2} + \frac{P\tan\theta_{voi}}{\omega_i \mathrm{V}_{orms}^2} \quad \mathrm{F} \quad (11)$$

where

$C_o^{'}$ is the capacitor for producing the current $\mathbf{I}_{C'}$;

$C_o^{''}$ is the capacitor for producing the current $\mathbf{I}_{C''}$;

P is the real power of load;

V_{orms} is the root mean square of output voltage.

3.4 Designing Example

This sub session show the guideline for designing the converter parameters. The assumption is that the converter system has input voltage 110 V_{rms}, frequency 50 Hz, and an induction motor load requires 220 V_{rms}, frequency 50 Hz to absorb power 1 kW at a lagging power factor 0.8. From this information, we design the converter parameters having the step as follows:

1. Finding the duty cycle;

$$D = (1 - 110\mathrm{V}_{rms} / 220\mathrm{V}_{rms}) = 0.5$$

2. Finding the load impedance;

$$R_o = \frac{\mathrm{V}_{orms}^2(\cos\theta_{iload})^2}{P} = 31 \ \Omega$$

and $L_o = \dfrac{R_O\tan\theta_{iload}}{2\pi\times 50} = 73$ mH

where $\theta_{iload} = \cos^{-1}0.8 = 36.8^o$

3. Finding the inductance value of *L*; the converter operates at 25 kHz and requires the inductor current ripple $\Delta i_L < 1\mathrm{V}$

$$L = \frac{\mathrm{V}_i \times D \times T_s}{\Delta i_L} = \frac{155\times 0.5\times 0.04\times 10^{-3}}{1} = 3.1 \text{ mH}$$

4. Finding the phase angle of output voltage using (8);

$$\theta_{vo} = 4^o$$

5. Using (11) to calculate C_o

$$C_o = 54 \ \mu\mathrm{F}$$

4. SIMULATION RESULTS

This session shows the simulation results to confirm the proposed technique. The converter parameters as shown in the designed step 1 – 5 are simulated by using Pspice program. The simulation results are illustrated in Fig. 5 - 8. Figure 5 (a) shows the load current and output voltage while Fig. 5 (b) shows the supply current and voltage. Although, load power factor is low at 0.8 lagging, the power factor at input side is unity. This is because of the optimal capacitance value of C_o $54\mu F$. Figure 6 (a) shows the variation of C_o affecting with input *PF*. When C_o is reduced or increased from the optimal capacitance value, this causes lagging or leading input *PF*, respectively. While Fig. 6 (b) shows the variation of duty cycle *D* versus input *PF*. At low *D*, the input *PF* is nearly unity, while at high *D*, the input *PF* is low. This is because of the effect of changing in phase angle of inductor current, θ_{iL}. However, this effect can be avoided by selecting the new capacitance value of C_o for the unity input *PF* at any *D* by using designed step 1 – 5.

In some cases of load impedance, the high ripple output voltage will be appeared at the output side because of small capacitance of C_o. For an example in this case, assuming that the load impedance is $Z_L = 50\Omega$. Using the designed step 1 – 5, the optimal capacitance value is $C_o = 5\mu F$. The simulation results are shown in Fig. 7 (a) causing high ripple output voltage although the input *PF* is unity as shown in Fig. 7 (b). To reduce the ripple output voltage, C_o should be increased. However, this causes a reduction in input *PF* as shown in Fig. 8. Therefore, in converter designing the designer should consider this effect, and also select C_o for the optimal ripple output voltage and input *PF*.

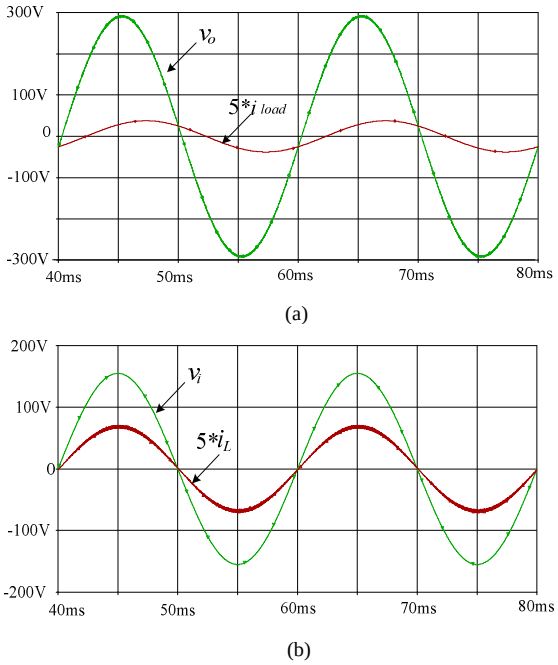

Fig. 5 Simulation results ($Z_L = 31 + j22.9\Omega$, $C_o = 54\mu F$, L = 3.1 mH, D = 0.5, and f_s = 25 kHz) (a) Output voltage and current; (b) Supply voltage and current.

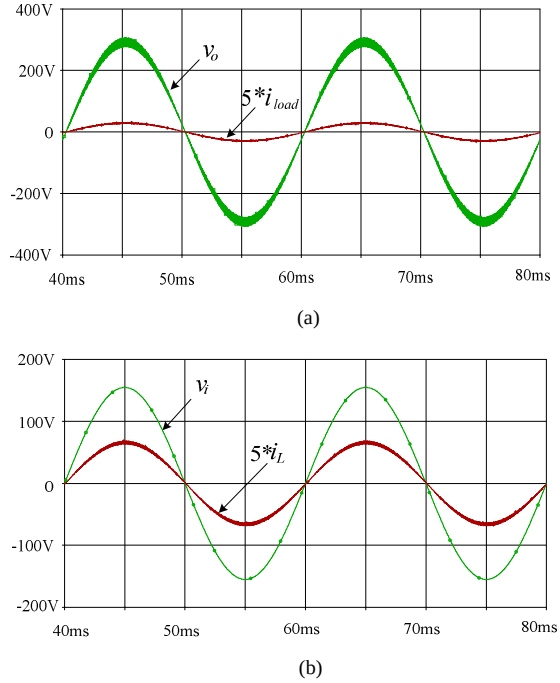

Fig. 7 Simulation results ($Z_L = 50\Omega$, $C_o = 5\mu F$, L = 3.1 mH, D = 0.5, and f_s = 25 kHz) (a) Output voltage and current; (b) Supply voltage and current.

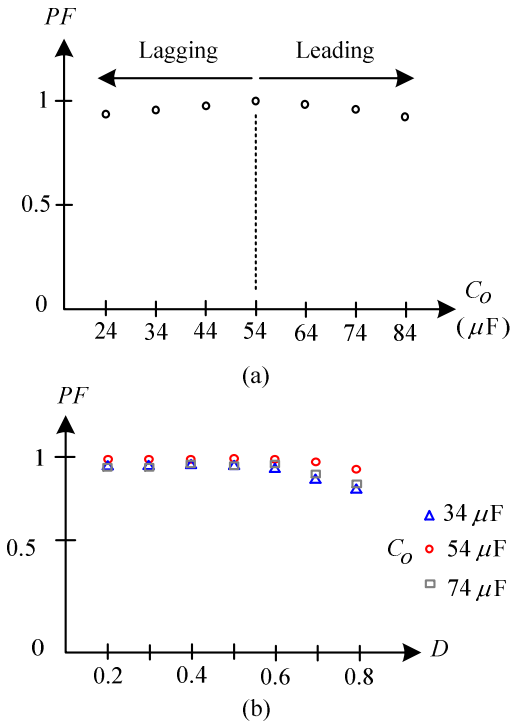

Fig. 6 Variation of input power factor ($Z_L = 31 + j22.9\Omega$, L = 3.1 mH and f_s = 25 kHz) (a) as a function of C_o, and (b) as a function of D.

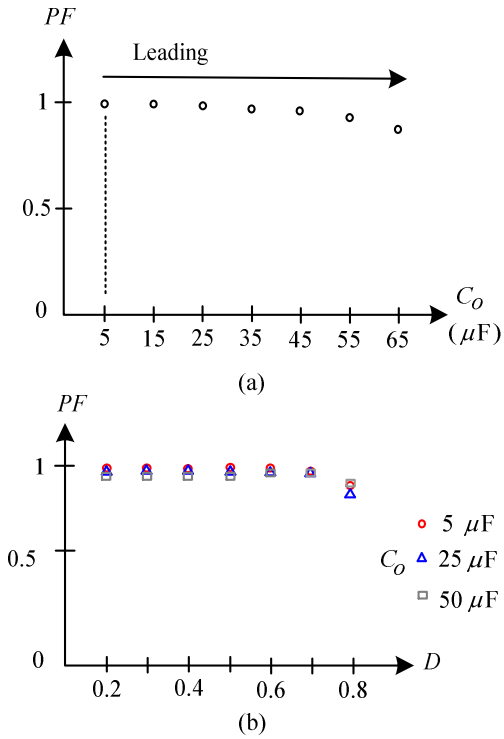

Fig. 8 Variation of input power factor ($Z_L = 50\Omega$, L = 3.1 mH, and f_s = 25 kHz) (a) as a function of C_o, and (b) as a function of D.

5. CONCLUSION

In this paper, we indicate that the capacitance value of C_o in PWM boost AC chopper topology affects the input power factor. To find the optimal capacitance value of C_o for AC chopper operation, therefore, we analyze the phase angles of supply current, output current and voltage. The simulation results show that the AC chopper can operate at the unity input power factor.

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