IETE Journal of Research
Publication details, including instructions for authors and subscription information:
http://www.tandfonline.com/loi/tijr20

Switching losses and harmonic investigations in multilevel inverters

Pradyumn K. Chaturvedi[a], Shailendra Jain[b], Pramod Agrawal[c], Rajesh K Nema[b] & Kaushal K Sao[d]

[a] Electrical Engineering Department, S.A.T.I., Vidisha MP 464001, India

[b] Electrical Engineering Department, MANIT, Bhopal MP 462052, India

[c] Electrical Engineering Department, IIT, Roorkee 247667, India

[d] Emerson Network Power (I) Ltd., Thane MH 400606, India

Published online: 01 Sep 2014.

To cite this article: Pradyumn K. Chaturvedi, Shailendra Jain, Pramod Agrawal, Rajesh K Nema & Kaushal K Sao (2008) Switching losses and harmonic investigations in multilevel inverters, IETE Journal of Research, 54:4, 297-307

To link to this article: http://dx.doi.org/10.4103/0377-2063.44233

Switching Losses and Harmonic Investigations in Multilevel Inverters

Pradyumn K. Chaturvedi, Shailendra Jain[1], Pramod Agrawal[2], Rajesh K. Nema[1] and Kaushal K. Sao[3]

Electrical Engineering Department, S.A.T.I., Vidisha (MP), 464 001 India.
[1]Electrical Engineering Department, MANIT, Bhopal (MP), 462 052 India.
[2]Electrical Engineering Department, IIT, Roorkee, 247 667 India.
[3]Emerson Network Power (I) Ltd., Thane, (MH), 400 606 India.

ABSTRACT

Use of conventional two-level pulse width modulation (PWM) inverters provide less distorted current and voltage but at the cost of higher switching losses due to high switching frequencies. Multilevel inverters are emerging as a viable alternative for high power, medium voltage applications. This paper compares total harmonic distortion and switching losses in conventional two-level inverters with multilevel inverters (three-level and five-level) at different switching frequencies. An optimized switching frequency has been obtained for a lower level of total harmonic distortion and switching losses. Diode-clamped, three-phase topology is considered for study. A sinusoidal PWM technique is used to control the switches of the inverter. Simulation study confirms the reduction in harmonic distortion and switching losses as the number of the levels increases.

Keywords:
Harmonics, Multilevel inverters, Pulse width modulation, Switching losses, Total harmonic distortion.

1. INTRODUCTION

Waveforms of practical inverters are non-sinusoidal and contain certain harmonics. For low- and medium-power applications, square wave or quasi-square wave voltage may be acceptable, but for high-power applications, sinusoidal waveforms with low distortion are required. Harmonic contents present in the output of a dc–ac inverter can be eliminated either by using a filter circuit or by employing pulse width modulation (PWM) techniques. Use of filters has the disadvantage of large size and cost, whereas use of PWM techniques reduces the filter requirements to a minimum or to zero depending on the type of application. Traditional two-level high-frequency PWM inverters have some drawbacks, such as production of common-mode voltages, more switching losses, requirement of switches with very low turn-on and turn-off times, large dv/dt rating, problem of voltage sharing in series connected devices and introduction of large amount of higher order harmonics [1-3].

Multilevel inverters have found better counterparts to the conventional two-level pulse width modulated inverters to overcome the above problems. In addition, they offer the advantage of less switching stress on each device for high voltage, high power applications, with a reduced harmonic content at low switching frequency.

A comparative study of three-level and five-level diode clamped, capacitor clamped and cascaded inverters has been presented in [4]. The effect of a passive LC filter on the inverter performance was studied. Simulation results indicate reduction in the total harmonic distortion (THD) by using higher number of levels. Switching losses become a dominant part of the total inverter losses at higher switching frequencies. Therefore, optimization of the switching frequency is necessary to reduce both THD and switching losses in the power devices. Switching frequency optimization was not considered in [4]. Switching losses and THD in three-level and five-level diode clamped inverters can also be optimized by using space vector PWM technique [5-7].

This paper investigates two-level inverters and three-level and five-level diode clamped three-phase inverters on the basis of the THDs and switching losses at different switching frequencies. An extensive simulation study to optimize the switching frequency based on the corresponding switching losses and THD contents in line voltage have been presented in this paper. A sinusoidal pulse width modulation (SPWM) technique is used for control.

Section 2 of the paper gives a system description of two-level, three-level and five-level inverters, whereas Section 3 presents the methodology for the switching loss calculation. Section 4 discusses the modulation techniques for two-level, three-level and five-level inverters and the last section compares these topologies on the

basis of switching losses and THD at different switching frequencies. Switching frequency optimization has been carried out to achieve a low level of both THD and switching loss.

2. BASICS OF TWO-LEVEL AND MULTILEVEL INVERTERS

2.1 Two-Level Inverters

This is the most widely used topology in various low- and medium-power applications. The full-bridge configuration of the three-phase voltage source inverter is shown in Figure 1. The switching logic to obtain output voltage for a 120^0 mode of operation is shown in Table 1. This topology can be used at a very high switching frequency to obtain low THD by using PWM techniques. Power devices are to be connected in series–parallel to achieve a large power capability. They suffer from static and dynamic voltage sharing problems in series and parallel connection of power devices, high rate of change of voltage due to synchronous commutation of series devices and inclusion of high switching frequency harmonic contents in inverter output voltage [3].

2.2 Multilevel Inverters

Multilevel inverters have grown as better counterparts to conventional two-level inverters. Commonly employed multilevel inverter topologies are Diode Clamped, Capacitor Clamped and Cascaded Multilevel inverters. In all these topologies, the output voltage is synthesized from several levels of input voltages obtained from several capacitors connected across the dc bus. In a capacitor clamped inverter, both real and reactive power can be controlled, but it suffers from higher switching losses due to real power transfer thus reducing the efficiency of power conversion. Also, it requires a large number of storage capacitors at higher levels. The cascaded inverter uses a large number of separate dc sources for each of the bridges. However, in the diode clamped topology, all devices are switched at the fundamental frequency resulting in low switching losses and high efficiency. Other main features of this topology are controlled reactive power flow between source and load, much better dynamic voltage sharing among switching devices and simple topological structure. Therefore, diode clamped inverter topology is considered here for study. The control logic is simple, especially for back-to-back inter-tie connections of two systems. However, it requires a large number of clamping diodes for a large number of output voltage levels. To produce an m-level output phase voltage, (m-1) switches are required for each half phase leg, a total of (m-1) dc link capacitors for energy storage and (m-1)*(m-2) clamping diodes for each phase leg [1-2].

2.2.1. Three-Level Diode Clamped Multilevel Inverter (DC-MLI)

Three-phase diode clamped three-level inverter (neutral point clamped) topology is shown in Figure 2. The circuit consists of two dc link capacitors, 12 power switches and six clamping diodes. The middle point of the dc bus capacitor is known as neutral point 'n'. The main feature of this topology is clamping diodes that clamp the switch voltage to half of the dc bus voltage, reducing the voltage stress of the switching device. The output voltage has three different states: +, 0 and – and the corresponding output phase voltages are $+V_{dc}/2$, 0 and $-V_{dc}/2$. Switching states to synthesize the output voltages for phase 'A' are defined in Table 2. A similar logic can be applied for the other two phases.

2.2.2. Five-Level DCMLI

The circuit diagram of the five-level DCMLI topology is shown in Figure 3. It consists of 24 power switches and 36 clamping diodes. The DC bus has four capacitors for a DC bus voltage V_{dc}. The voltage across each capacitor

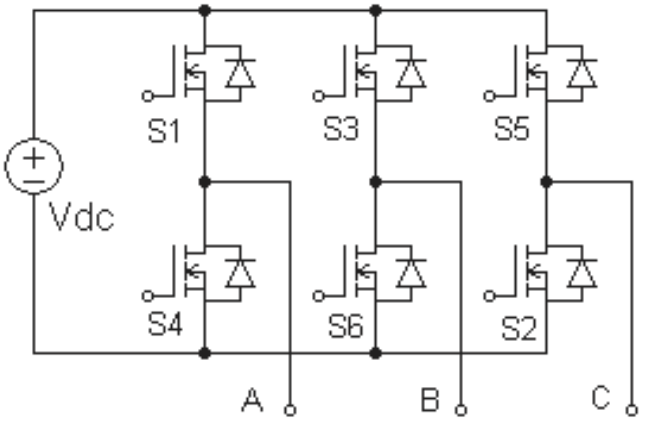

Figure 1: Three-phase two-level inverter.

Table 1: Switching states of a two-level three-phase inverter

Load line voltage (V_{AB})	Switching states					
	S_1	S_2	S_3	S_4	S_5	S_6
$+V_{dc}/2$	1	0	0	0	0	1
$+V_{dc}/2$	1	1	0	0	0	0
0	0	1	1	0	0	0
$-V_{dc}/2$	0	0	1	1	0	0
$-V_{dc}/2$	0	0	0	1	1	0
0	0	0	0	0	1	1

Table 2: Switching states for phase 'A' of a three-level diode clamped inverter

S_{a1}	S_{a2}	S'_{a1}	S'_{a2}	Switching states	Output pole voltage (V_{Ao})	Output phase voltage (V_{An})
1	1	0	0	+	$+V_{dc}$	$+V_{dc}/2$
0	1	1	0	0	$+V_{dc}/2$	0
0	0	1	1	-	0	$-V_{dc}/2$

is $V_{dc}/4$; thus, the voltage stress across each device will be limited to $V_{dc}/4$ through the clamping diode. Table 3 shows the switching combinations and corresponding output phase voltage levels where switching state '1' represents the switch is in 'on' condition and state '0' indicates the switch is in 'off' condition. When the number of levels is high enough in the DCMLI, harmonic contents in the output voltage and current get reduced to avoid the need for filters.

3. SWITCHING LOSS CALCULATIONS

Consider a single MOSFET switch connected across a dc voltage of value V_{dc}. Current through switch during 'on' time is considered as I_{dc}. Figure 4 shows the waveforms of the voltage across and the current through the switch when it is operated at a switching frequency of $F_s = 1/T_s$, where T_s is the switching period. To simplify the expressions, the switching waveforms are represented by linear approximations. In the figure, v_M and i_M are the voltage across and the current through the MOSFET [3, 5].

Switching losses can be calculated from the turn-on and turn-off characteristics of the devices. Instantaneous voltage and current during turn on time $t_{c(on)}$ are

$$v(t) = V_{dc} - (V_{dc} - V_{on})*(t/t_{c(on)}); \qquad 0 < t \le t_{c(on)} \tag{1}$$

$$i(t) = I_{dc} * (t/ t_{c(on)}); \qquad 0 < t \le t_{c(on)} \tag{2}$$

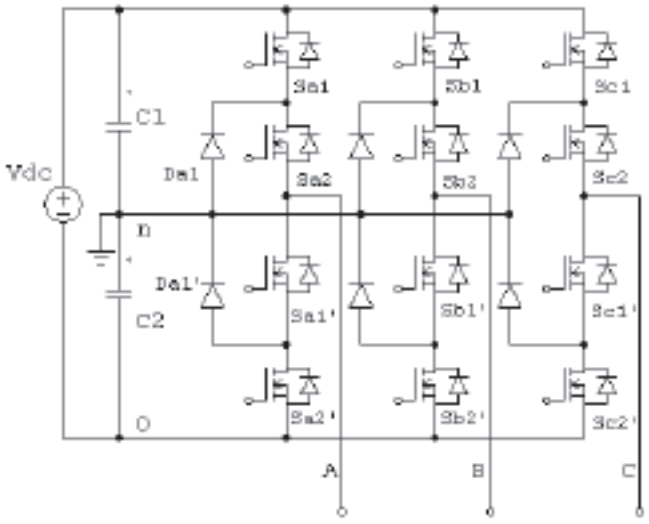

Figure 2: Three-phase three-level diode clamped inverter.

Instantaneous power during the interval $t_{c(on)}$ is

$$p(t) = v(t)*i(t)$$

$$=\{V_{dc} - (V_{dc} - V_{on})*(t/t_{c(on)})\}* \{I_{dc} * (t/ t_{c(on)})\}$$

$$=\{V_{dc} *I_{dc} * (t/ t_{c(on)}) \} - (V_{dc} - V_{on})*(t^2/t_{c(on)}^2) \tag{3}$$

and energy dissipated during this interval is $t_{c(on)}$,

$$E_{c, on} = \int[\{V_{dc} *I_{dc} *(t/ t_{c(on)})\} - (V_{dc} - V_{on})*(t^2/t_{c(on)}^2)]\, dt \quad 0 \text{ to } t_{c(on)}$$

$$E_{c, on} = (V_{dc} *I_{dc} * t_{c(on)})/2 - (V_{dc} - V_{on})* I_{dc} * t_{c(on)}/3$$

$$= (V_{dc} *I_{dc} * t_{c(on)})/6 - (V_{on} * I_{dc} * t_{c(on)})/3 \tag{4}$$

and during turn-off transition, of $t_{c(off)}$, the current falls from I_{dc} to zero and the V_{on} rises linearly to V_{dc}. The instantaneous voltage and current during this period are

$$v(t) = V_{on} + (V_{dc} - V_{on})/t_{c(off)} \tag{5}$$

$$i(t) = I_{dc} - I_{dc}/t_{c(off)} \tag{6}$$

The instantaneous power dissipated during the interval $t_{c(off)}$ is

$$p(t) = v(t)*i(t)$$

$$= \{V_{on} + (V_{dc} - V_{on})*(t/t_{c(off)})\}* \{ I_{odc} - I_{dc} * (t/ t_{c(off)})\}$$

$$= V_{on} *I_{dc} + (V_{dc} - V_{on})*I_{dc} *(t/t_{c(off)}) - V_{on} *I_{dc} *(t/t_{c(off)}) -$$

$$(V_{dc} - V_{on})*I_{dc} *(t^2/t_{c(off)}^2) \tag{7}$$

Hence, the energy dissipated can be found as $t_{c(off)}$,

$$E_{c, off} = \int[V_{on} *I_{dc} + (V_{dc} - V_{on})*I_{dc} *(t/t_{c(off)}) - V_{on} *I_{dc}$$

$$*(t/t_{c(off)}) - (V_{dc} - V_{on})*I_{dc} *(t^2/t_{c(off)}^2)]\, dt \qquad 0 t_{c(on)}$$

$$= (V_{dc} *I_{dc} *t_{c(off)})/6 - (V_{on} *I_{dc} *t_{c(off)})/3 \tag{8}$$

With a switching frequency of F_s, the average switching loss in the switch during each transition of turn on and turn off can be found as

$$P_{c, on} = (V_{dc} *I_{dc} *t_{c(on)}/T_s)/6 + (V_{on} *I_{dc} *t_{c(on)}/T_s)/3 \tag{9}$$

$$P_{c, off} = (V_{dc} *I_{dc} *t_{c(off)}/T_s)/6 - (V_{on} *I_{dc} *t_{c(off)}/T_s)/3 \tag{10}$$

Hence, the average switching loss P_{sw} in the switch is

$$P_{sw} = (1/6)*V_{dc} *I_{dc} *\{t_{c(on)} + t_{c(off)}\}/T_s + (1/3)*V_{on} *I_{dc} *\{t_{c(on)} + t_{c(off)}\}/T_s \tag{11}$$

Table 3: Switching states for phase 'A' of a five-level diode clamped inverter

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S'_{a1}	S'_{a2}	S'_{a3}	S'_{a4}	Output phase voltage (V_{An})	Output pole voltage (V_{Ao})
1	1	1	1	0	0	0	0	$+V_{dc}/2$	V_{dc}
0	1	1	1	1	0	0	0	$+V_{dc}/4$	$3V_{dc}/4$
0	0	1	1	1	1	0	0	0	$V_{dc}/2$
0	0	0	1	1	1	1	0	$-V_{dc}/4$	$V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$	0

Eqn. (11) shows that the switching power loss in a semiconductor switch varies linearly with the switching frequency and switching times. Therefore, with the devices having short switching times, it is possible to operate them at a higher switching frequency thus avoiding excessive switching power losses in the device [8-10].

Nomenclature of variables used are given in Appendix-I

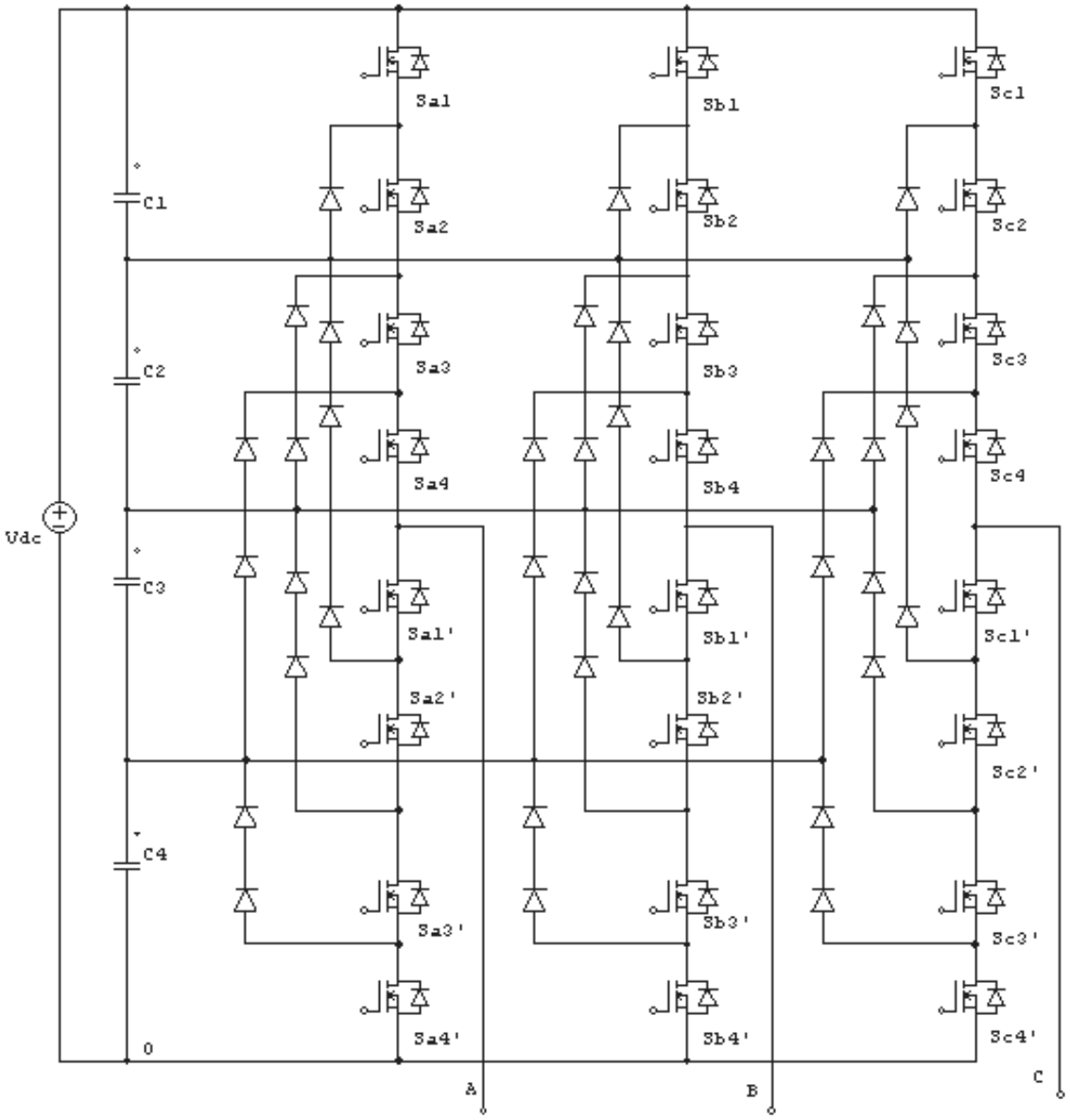

Figure 3: Three-phase five-level diode clamped inverter.

Appendix I: Nomenclature

v(t), i(t), p(t)	instantaneous voltage, current and power	$P_{c,on}$, $P_{c,off}$	average switching loss during $t_{c(on)}$ and $t_{c(off)}$
V_{dc}	voltage across switch when turned-off	T_s	sampling time in sec
V_{on}	voltage across switch when turned-on	F_s	switching frequency in Hz
t	time in sec	P_{sw}	average switching loss in watts
$t_{c(on)}$	turn-on cross-over interval	$t_{d(on)}$	turn-on delay time
I_{dc}	current through switch when turned-on	$t_{ri,on}$	turn-on current rise time
$E_{c,on}$	energy dissipated during turn-on cross-over interval	$t_{fv,on}$	turn-on voltage fall time
$t_{c(off)}$	turn-off cross-over interval	$t_{d(off)}$	turn-off delay time
$E_{c,off}$	energy dissipated during turn-off cross-over interval	$t_{rv,off}$	turn-off voltage rise time
		$t_{fi,off}$	turn-off current fall time

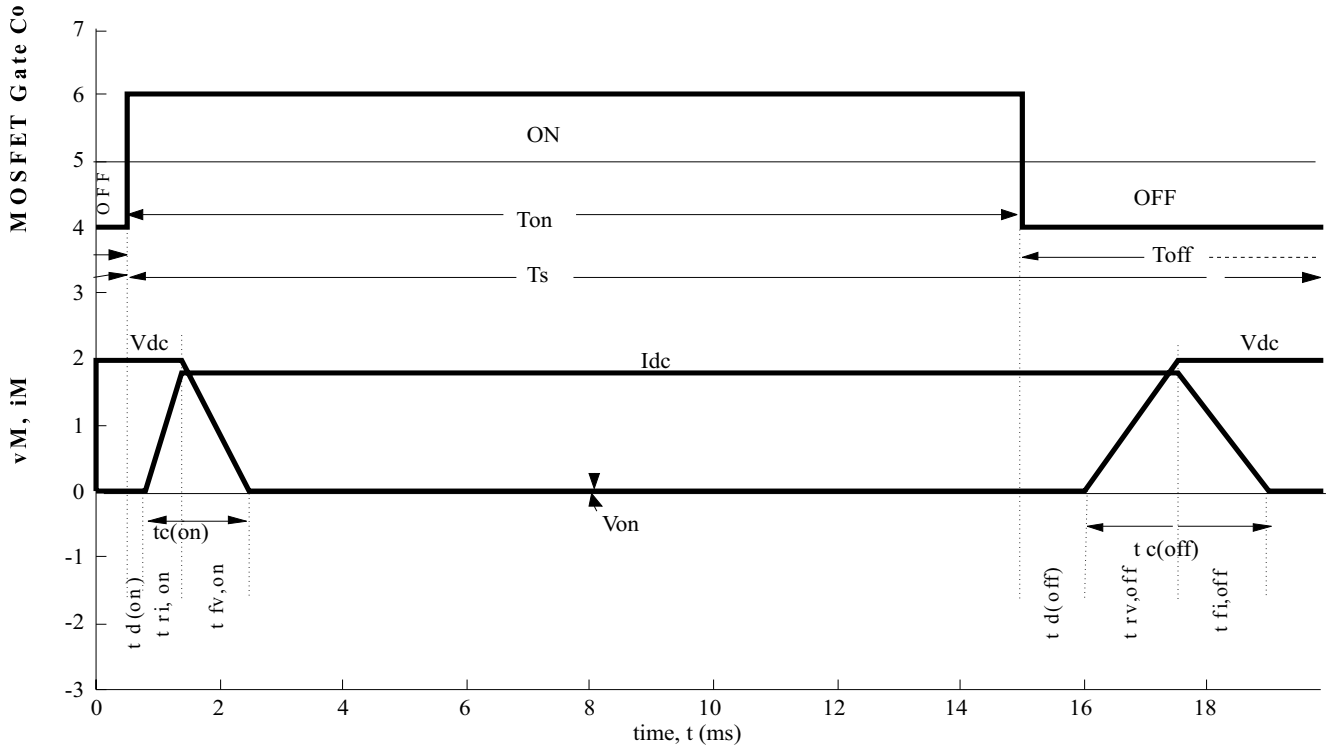

Figure 4: Linearized switching characteristics.

whereas load parameters considered for simulation study are given in Appendix-II.

4. MODULATION TECHNIQUE

Modulation techniques for voltage source inverters may be carrier based or carrier-less and open loop or closed loop. These modulation or control techniques for multilevel voltage source inverters are classified in Figure 5. Simulation investigation of different multilevel control techniques have been presented in [11]. The SPWM technique is considered for study in this paper. It is the simple technique to be implemented. In the SPWM technique, a triangular carrier wave at a high switching frequency is compared with the sinusoidal reference wave at a fundamental output frequency. The SPWM technique is again divided into Alternate Phase Opposition Disposition, Phase Opposition Disposition and In Phase (PH) [12].

Figure 6 shows the generation of switching pulses for power device S_1 of the two-level inverter shown in Figure 1. One triangular carrier wave is compared with a sinusoidal reference wave to generate switching pulses. For power device S_4, the complementary of this pulse is to be given. The control principle of the SPWM is to use several triangular carrier signals keeping only one modulating sinusoidal signal. If an m-level inverter is employed, (m-1) level shifted carriers will be needed.

Appendix II: Simulation parameters

Load parameters	MOSFET parameters	
Three-phase active	$t_{c(on)}$	48 ns
power 8 kW	$t_{d(on)}$	15 ns
Three-phase inductive	$t_{ri, on}$	25 ns
reactive power 6 kVar	$t_{c(off)}$	85 ns
Nominal frequency 50 Hz	$t_{d(off)}$	52 ns
Nominal phase-phase	$t_{fi, off}$	25 ns
voltage		200 Volts

ns: nanoseconds

Two and four triangular carrier signals are needed for three- and five-level inverters, respectively. The carriers have the same frequency f_c and the same peak-to-peak amplitude A_c. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency f_m and amplitude A_m. At every instant, each carrier is compared with the modulating signal. Each comparison switches the switch 'on' if the modulating signal is greater than the triangular carrier assigned to that switch. Obviously, the actual driving signals for the power devices can be derived from the results of the modulating–carrier comparison by means of a control logic circuit. Figure 7 shows the generation of switching pulses for power devices S_{a1} and S_{a2} of the three-level inverter shown in Figure 2. Pulses for the lower two devices S_{a1}' and S_{a2}' are complementary to these pulses,

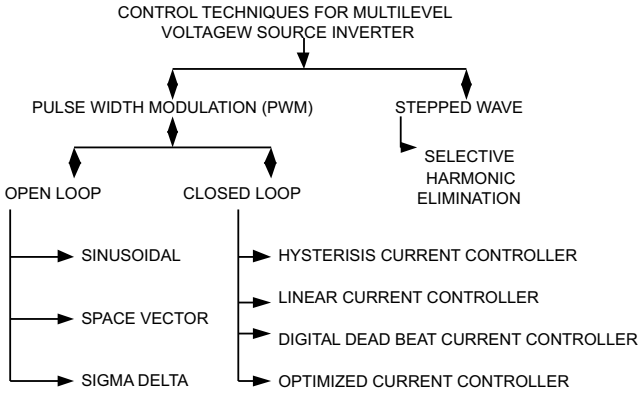

Figure 5: Classification of multilevel control techniques [12].

respectively. Figure 8 shows the generation of switching pulses for power devices S_{a1}, S_{a2}, S_{a3} and S_{a4} of the five-level inverter shown in Figure 3. Pulses for the lower four devices S_{a1}', S_{a2}', S_{a3}' and S_{a4} are complementary to these pulses, respectively. V_r is the reference sin wave and V_{t1}, V_{t2}, V_{t3}, V_{t4} are four carrier signals.

5. SIMULATION STUDY OF DCMLI WITH SPWM

After modelling the control logic of the SPWM technique as discussed in section 4, simulation studies have been performed on two-level, three-level and five-level diode clamped three-phase inverters. The output voltage waveform and its frequency spectrum for a two-level inverter at a switching frequency of 1 kHz are shown in Figure

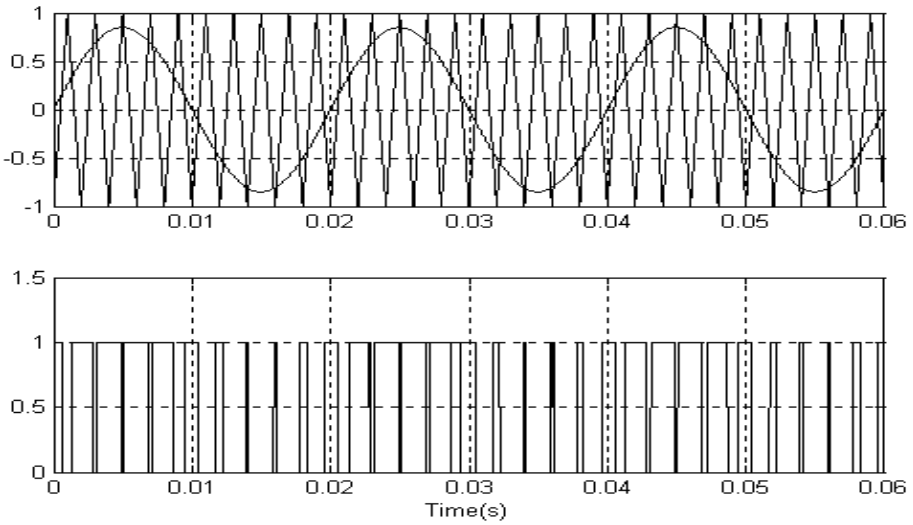

Figure 6: Pulse generation for two-level inverter (for switch S_1).

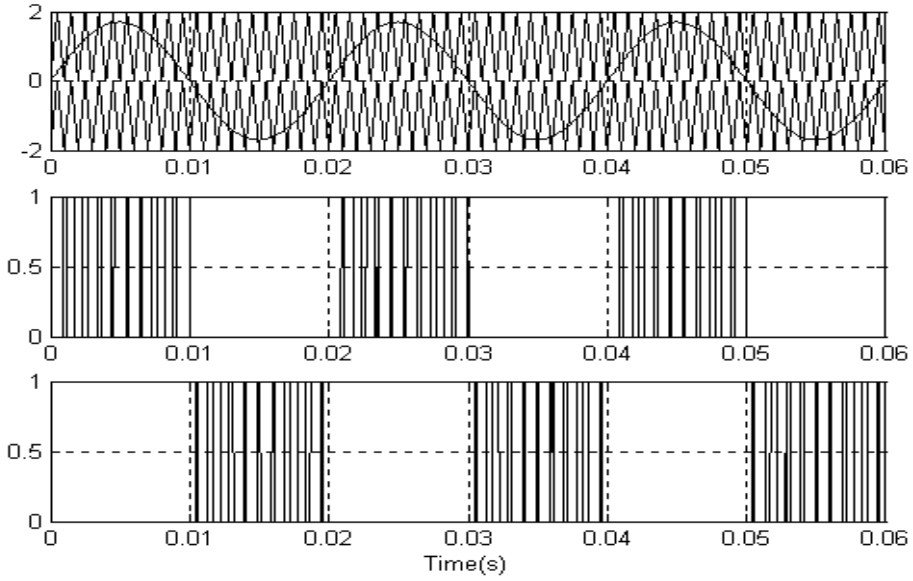

Figure 7: Pulse generation for three-level inverter (for switches Sa_1 and Sa_2).

9. Table 4 gives the THD and switching losses in each phase voltage at different switching frequencies. As the switching frequency is increased THD is reduced. The total switching losses are calculated as discussed in section 3, and tabulated in Table 5 for the different carrier frequencies ranging from 1500 to 5000 Hz.

It can be observed from Table 4 that a decrease in the carrier frequency results in a lower value of switching losses. This is due to the reduced number of 'sampling points' at reduced carrier frequencies, which in turn limit the number of switching transitions in one PWM switching cycle, resulting in lower switching losses. Lowering the value of the carrier frequency still preserves the average shape of the fundamental 50 Hz sinusoidal but exhibits an increase in the THD due to increased 'notches' within the width of each generated output pulse. To locate the optimum point whereby both THD and switching losses are optimized, the performance of the two-level converter is observed at several carrier frequencies and the values of THD and switching losses are noted.

From the values of THD and switching losses obtained, a graph of THD and switching losses with reference to carrier frequencies is constructed to locate the optimum point with minimized losses, as shown in Figure 10. From Figure 10 it is clear that at the switching frequency of 2300 Hz, THD and switching losses are optimized.

Table 4: THD and switching losses for a two-level inverter at different switching frequencies

Carrier frequency (Hz)	% THD			Total switching losses (mJ)
	Phase A	Phase B	Phase C	
1500	44.26	44.35	44.82	25.80
2500	40.48	40.73	40.63	47.68
3500	37.56	37.42	37.61	62.35
5000	31.83	31.54	31.67	88.18

THD: Total harmonic distortion

Table 5: THD and switching losses for a three-level inverter at different switching frequencies

Carrier frequency (Hz)	% THD			Total switching losses (mJ)
	Phase A	Phase B	Phase C	
1500	34.10	34.13	33.94	21.88
2500	22.05	22.39	22.52	31.86
3500	14.68	14.93	14.89	39.40
5000	8.97	8.64	9.16	46.64

THD: Total harmonic distortion

Table 6: THD and switching losses for the five-level inverter at different switching frequencies

Carrier frequency (Hz)	% THD			Total switching losses (mJ)
	Phase A	Phase B	Phase C	
1500	25.94	25.66	24.93	13.42
2500	19.18	19.64	20.21	19.47
3500	8.18	8.83	8.44	26.60
5000	6.31	5.37	5.84	33.33

THD: Total harmonic distortion

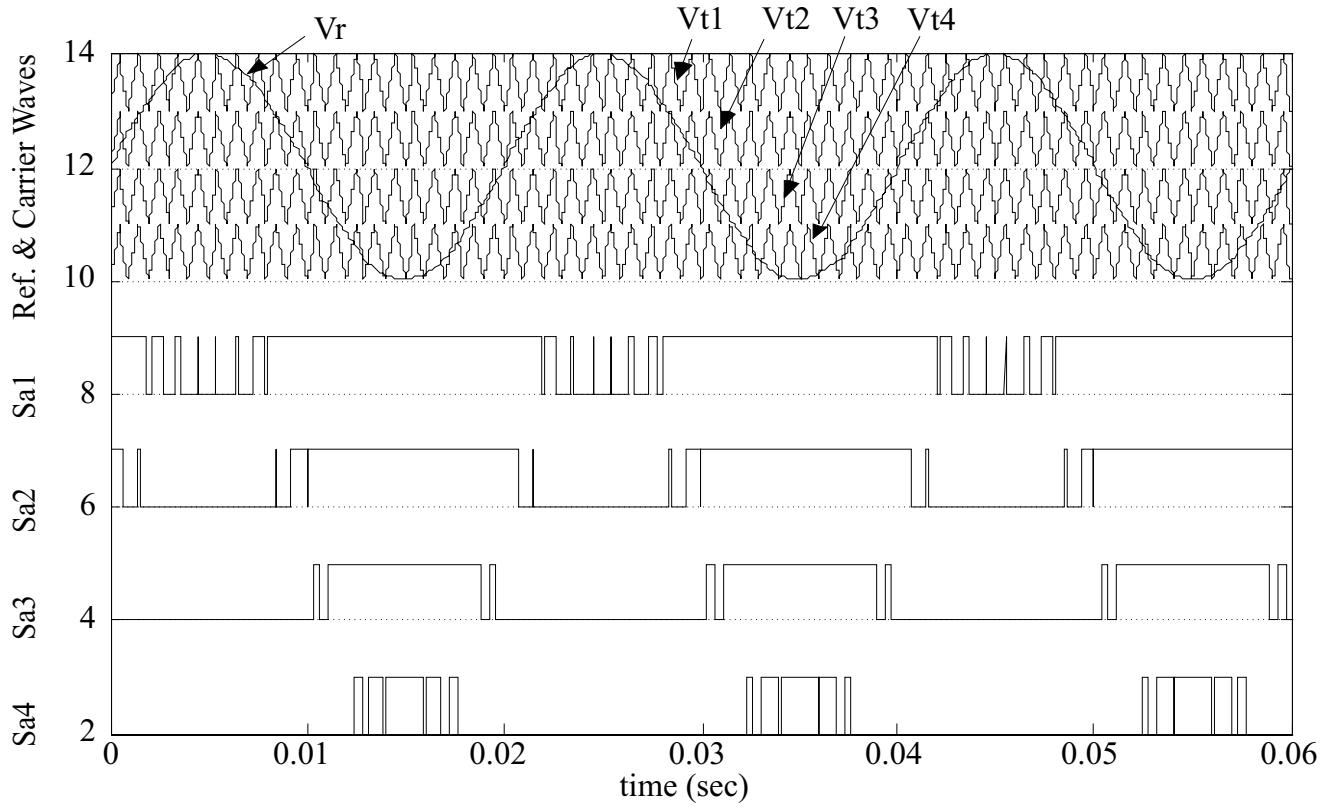

Figure 8: Pulse generation for five-level inverter (for switches Sa_1, Sa_2, Sa_3 and Sa_4).

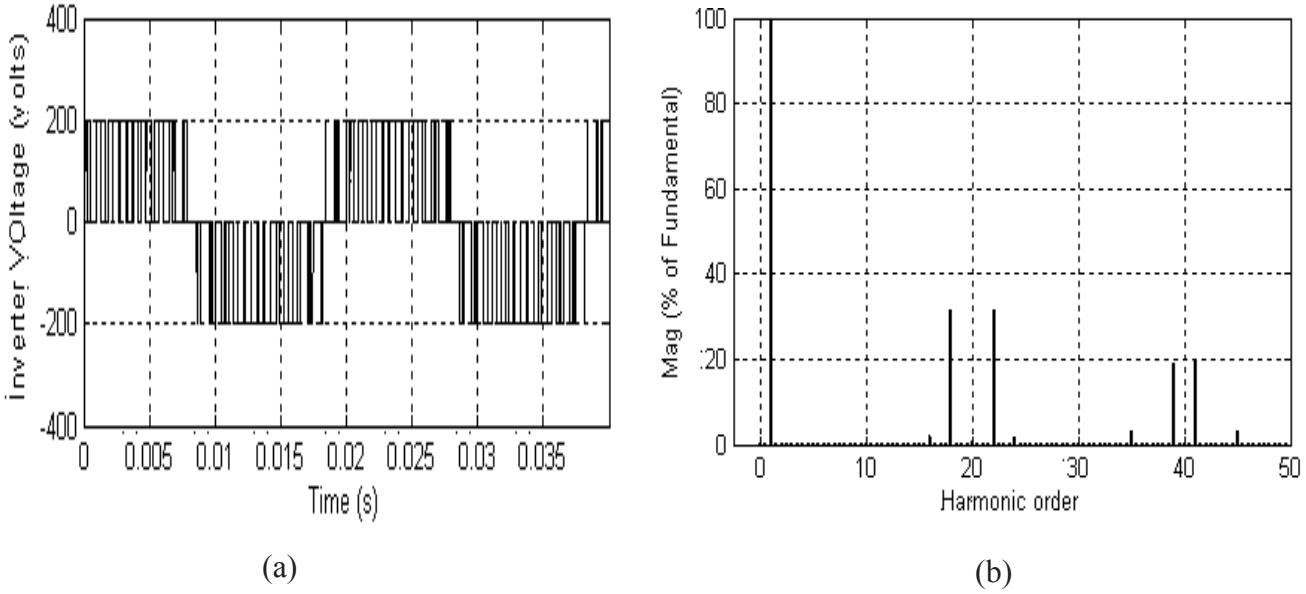

Figure 9: Output voltage of two-level inverter and its frequency spectrum.

Output voltage waveform and its frequency spectrum for the three-level inverter at a switching frequency of 1 kHz are shown in Figure 11. The THD and the total switching losses are calculated and tabulated in Table 5 for different carrier frequencies ranging from 1500 to 5000 Hz. From the simulation results and analysis taken for the three-level three-phase inverter, it is observed that with the increase in the number of levels, the system performance is improved in terms of the THD and switching losses. The voltage impressed across the terminals of the switches is reduced from 200 to 100 volts as compared to the two-level inverter. However, it is also observed that an unequal device rating would be necessary for the three-level inverter.

To obtain the output voltage corresponding to that of V_{dc} of the input voltage, both switches S_{a1} and S_{a2} have to be turned on. However, to produce the level of $0.5V_{dc}$, switch S_{a2} remains on while S_{a1} turns off. It shows that switch S_{a2} remains on for one switching sequence more than that of S_{a1} and S_{a2} conducts over the entire cycle except when the output voltage is equal to zero. Such unequal conduction duty requires different ratings for the switching devices. When the inverter is designed to use the average duty for all devices, the outer switches may be oversized and the inner switches may be undersized. Because of this reason, it is observed that switching losses were considerably reduced as compared with that of the two-level inverter.

According to Table 5, switching losses were reduced to almost half with a decrease in the switching frequency from 5000 to 1500 Hz. However, this is achieved at an

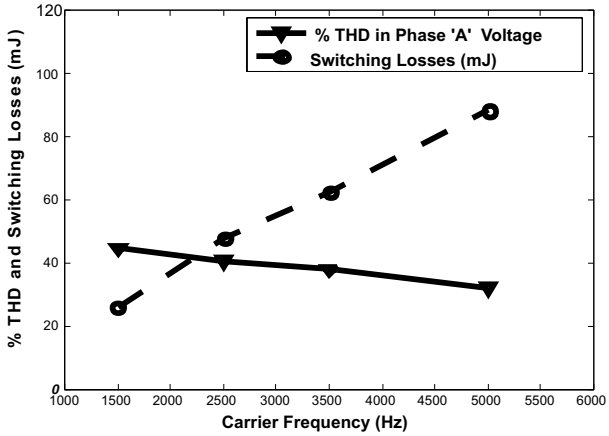

Figure 10: Variation of switching losses and THD with carrier frequency for the two-level inverter.

expense of an increase in the THD level. For different carrier frequencies, the switching loss and THD levels associated with different carrier frequencies were observed and a graph of variation of THD and switching loss with carrier frequency is constructed to locate the optimum point, as shown in Figure 12.

The output voltage and its frequency spectrum of a five-level inverter at a switching frequency of 1 kHz are shown in Figure 13. The system performance for the five-level inverter is further improved in terms of the THD and switching losses. The voltage impressed across the terminals of the switches is further reduced to 50 volts from 200 volts as in the two-level inverter. However, it is also observed that unequal device rating would be

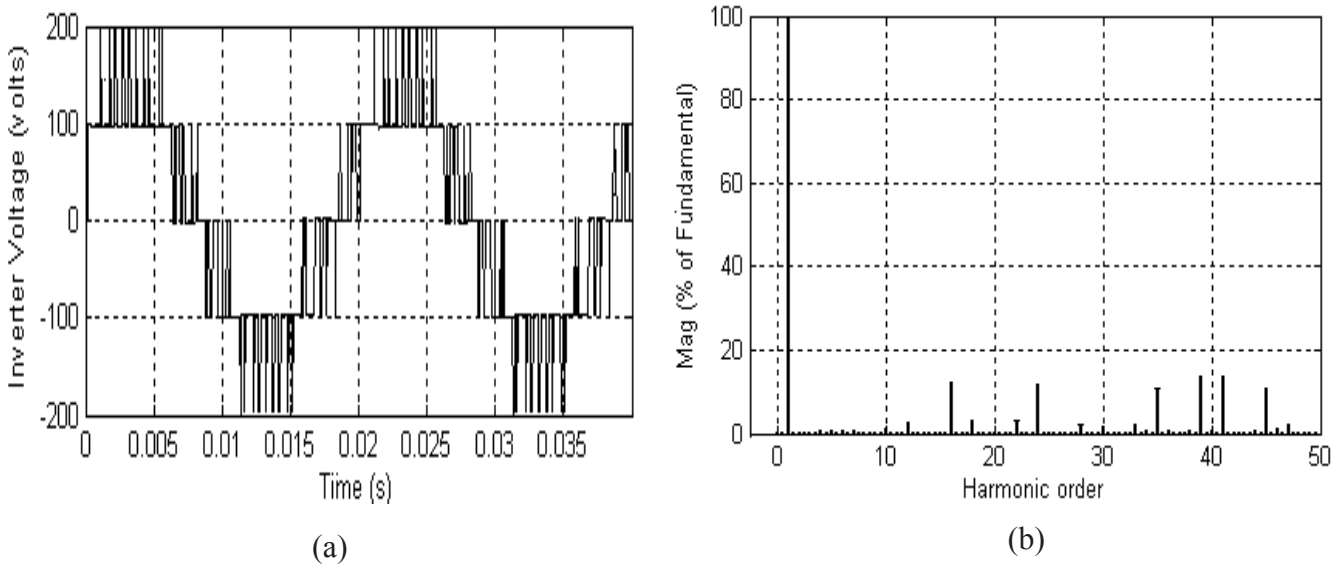

Figure 11: Output voltage of the three-level inverter and its frequency spectrum.

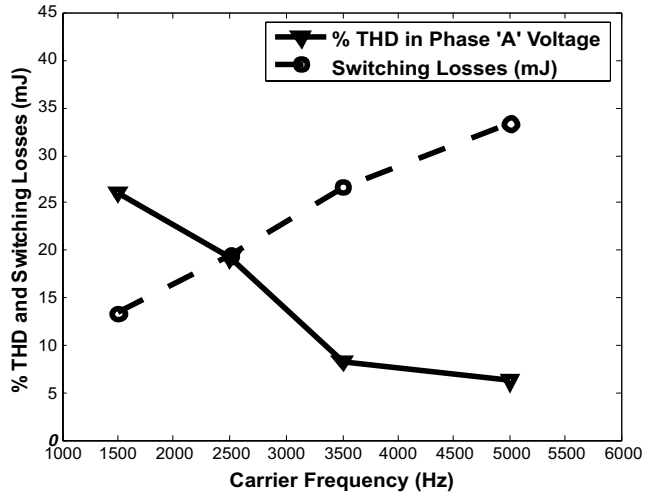

Figure 12: Variation of switching losses and THD with carrier frequency for the three-level inverter.

necessary for the five-level inverter as well, similar to that of the three-level topology. From Table 3, it can be seen that to obtain an output voltage corresponding to that of V_{dc} of the input voltage, all top switches have to be turned on. However, to produce the level of $0.75V_{dc}$, switches S_{a2}, S_{a3} and S_{a4} remain on while S_{a1} turns off and its complement S_{a1}' turns on. This continues until a voltage output of $0.5V_{dc}$ is required, which in turn causes S_{a2} to turn off and its complement S_{a2}' to be turned on. When a voltage level of $0.25V_{dc}$ is needed, S_{a3} turns off while S_{a4} remains on. Hence, it can be seen that S_{a4} remains on for three switching sequences allowing it to conduct over the entire cycle except when the output voltage required is zero. Such unequal conduction duty cycle requires the switches to be sized differently in terms of both their current and their voltage ratings. When the inverter design is to use the average duty for all devices, the outer switches may be oversized and the inner switches may be undersized as in the three-level inverter.

Table 6 shows the total switching losses and % THD in each phase voltage for different carrier frequencies ranging from 1500 to 5000 Hz for a five-level inverter. It is noted that switching losses are considerably reduced than that of the two-level and three-level inverters mainly due to the fact that the voltage across the terminals of the switch is considerably lesser.

Variation of THD and switching losses for different carrier frequencies is constructed to locate the optimum point, as shown in Figure 14. Figures 15 and 16 show the variation of switching losses and THD for two-level, three-level and five-level inverters, respectively. It is observed that switching losses reduce with increased number of levels in output voltage at a particular switching frequency. However, for the same inverter level, switching losses increase with switching frequency. It is clear from Figure 16 that THD reduces with number of inverter levels and also with switching frequency.

6. CONCLUSION

A comparative study of THD of the output voltage waveform and switching losses of two-level, three-level and five-level three-phase diode clamped inverters has been presented in this paper using the SPWM technique. It has been observed that both THD and switching losses decrease with the increase in the number of levels in the output voltage. However, with the decrease in carrier frequency, the THD level increases and switching losses

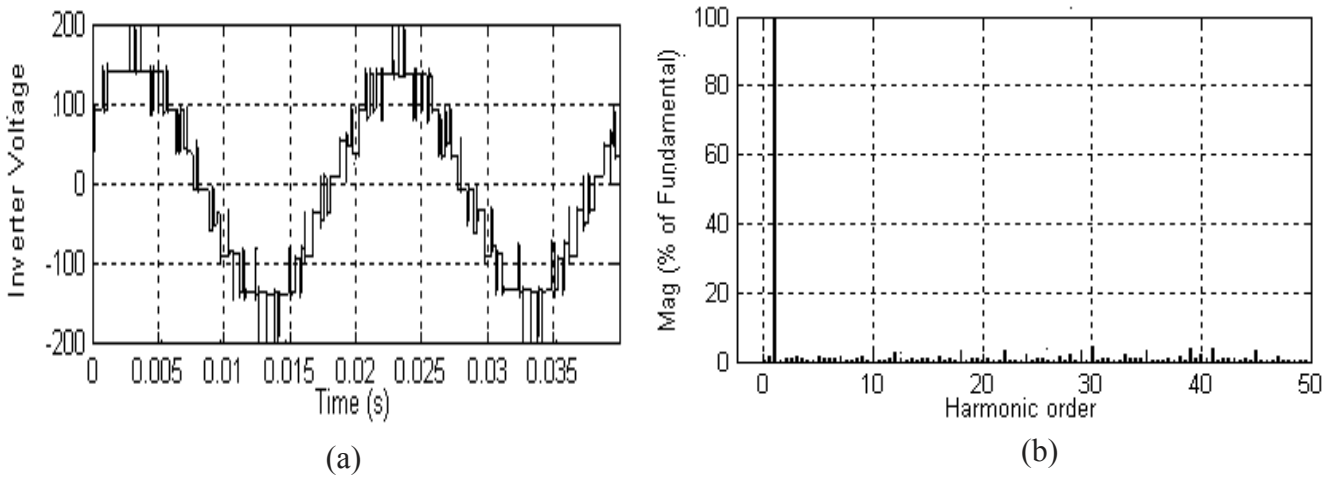

Figure 13: Output voltage of a five-level inverter and its frequency spectrum.

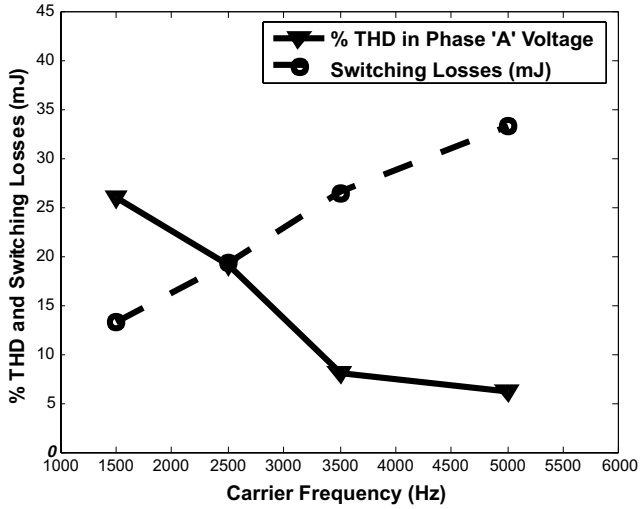

Figure 14: Variation of switching losses and THD with carrier frequency for a five-level inverter.

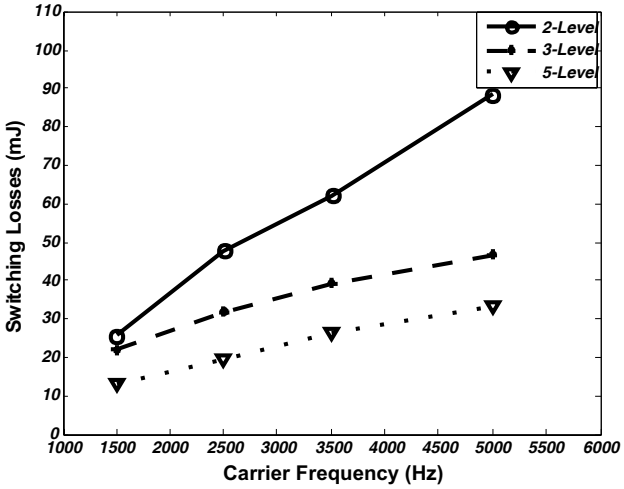

Figure 15: Variation of switching losses for two-level, three-level and five-level inverters with carrier frequency.

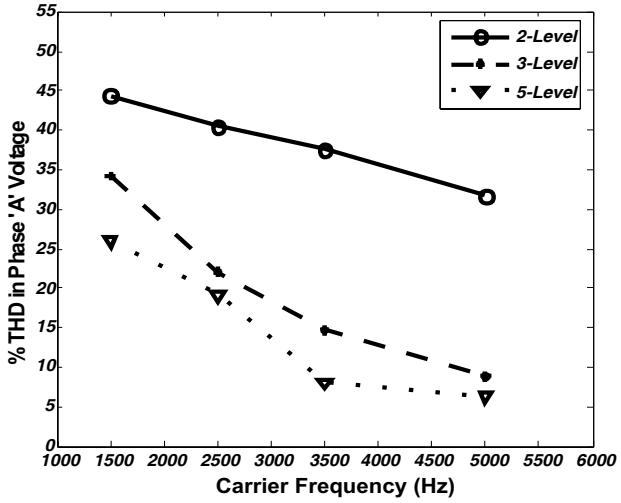

Figure 16: Variation of percentage THD for two-level, three-level and five-level inverter with carrier frequency.

reduce proportionately. Figures 10, 12 and 14 can be referred to optimize the switching losses and harmonic contents for operation of an inverter at an optimized switching frequency. The above investigation is made without an output filter. By using suitable filters, the harmonic content can be further reduced.

REFERENCES

1. F. Z. Peng & J. S. Lai, 'Multilevel Converters - A new breed of power converters', *IEEE Transaction on Industry Applications*, Vol. 32, No. 3, May/June, 1996, pp. 509-517.
2. Jose Rodriguez, J. S. Lai & F. Z. Peng, 'Multilevel Inverters: A Survey of Topologies, Controls, and Applications', *IEEE Transaction on Industrial Electronics*, Vol. 49, No. 4, Aug 2002, pp. 724-738.
3. Mohan Ned, Undeland T.M. & Robbins W.P., 'Power Electronics: Converters, Applications and Design', John Wiley and Sons, Second Edition, 2001.
4. G. Bhuvaneswari & Nagaraju, 'Multilevel Inverters - A Comparative Study', *IETE Journal of Research*, Vol. 51, No.2, Mar-Apr 2005, pp.

141-153.

5. B. Kaku, I. Miyashita & S. Sone, 'Switching Loss Minimized Space Vector PWM Method for IGBT Three-Level Inverter', *IEE Proceedings, Electric Power Applications*, Vol. 144, No. 3, May 1997, pp 182-190.
6. Markku Jokinen & Anssi Lipsanen, 'Fundamental Study of 2-Level and 3-Level frequency Converters', Assignment on converter Losses, SMOLA, Norway, 2005.
7. Trzynadlowski A. M., 'Space Vector PWM Technique with Minimum Switching Losses and a Variable Pulse Rate', *Conference Proceedings of IECON* 1993, pp. 689-694.
8. Richard Lund, Jonas B., Sigurd O. & Roy Nilsen, 'Analytical Power Loss Expressions for diode Clamped Converters', *EPE-PEMC*, Dubrovnik and Cavtat, 2002.
9. A.D. Rajapakse, A.M. Gole & P.L. Wilson, 'Approximate Loss Formulae for Estimation of IGBT Switching Losses through EMTP-type Simulations', *IPST-2005*, Montreal, Canada, Jun 19-23, 2005, Paper no, IPST05-184.
10. Alain Laprade & Ron H. Randall, 'Numerical Method for Evaluating IGBT Losses', *Application Notes, Fairchild Semiconductors*, Jan 2000, AN-7520.
11. P. K. Chaturvedi, Shailendra K. Jain, Pramod Agrawal & P. K. Modi, 'Investigations on Different Multilevel Inverter Control Techniques by Simulation', *PEDES-2006*, New Delhi, 12-15 Dec 2006, CD Rom, Paper No 3C-12.
12. Massoud A.M., Finney S.J. & Williams B.W., 'Control techniques for multilevel voltage source inverters', *34th Power Electronics Specialist Conference*, Jun 15-19, 2003, Vol - I, pp. 171-176.

AUTHORS

Pradyumn K. Chaturrvedi received B.E. degree in Electrical Engg and M.E. degree in Power Electronics from Samrat Ashok Technological Institute, Vidisha (MP), India, in 1996 and 2001 respectively. He has been with the department of Electrical Engineering as Lecturer at Samrat Ashok Technological Institute, Vidisha (MP), India. Currently, he is working towards Ph.D. degree at Maulana Azad National Institute of Technology (Deemed University), Bhopal, India. His fields of interest are electrical drives, high power factor converters and multilevel inverters.

E-mail: pradyumnc74@rediffmail.com

Shailendra Jain received the B.E. degree from Samrat Ashok Technological Institute, Vidisha, India, in 1990, the M.E. degree from Shri Govindram Seksaria Institute of Technology and Science, Indore, India, in 1994, and the Ph.D. degree from the Indian Institute of Technology, Roorkee, India, in 2003. He was a Post Doctorate Fellow at University of Western Ontario, Canada in 2007. Currently, he is Assistant Professor in the Department of Electrical Engineering at Maulana Azad National Institute of Technology (Deemed University), Bhopal, India. His fields of interest include power electronics, electrical drives, active power filters, Fuel Cell technology and high power factor converters.

E-mail: shailjain02@rediffmail.com

Pramod Agarwal received the B.E., M.E., and Ph.D. degrees in electrical engineering from the University of Roorkee, Roorkee, India, in 1983, 1985, and 1995, respectively. Currently, he is Professor in the Electrical Engineering Department at the Indian Institute of Technology, Roorkee, India. He was a Lecturer in the Department of Electrical Engineering at the University of Roorkee in 1985 and became an Assistant Professor in 1996. He was a Post-Doctoral Fellow at the University du Quebec, Montreal, QC, Canada, from 1999 to 2000. He has guided more than 50 B.E. and 25 M.E. projects, and published many papers in various national and international journals and conferences. He has developed a number of educational units for laboratory experimentation. His fields of specialization are electrical machines, power electronics, microprocessor- and microcomputer-controlled ac/dc drives, active power filters, and high power factor converters.

E-mail: pramgfee@iitr.ernet.in

Rajesh K. Nema has received his PhD degree in Electrical Engineering from Barkatullah University, Bhopal, India in 2004. He completed his M.Tech in Heavy Electrical Equipments in 1992 and degree of Bachelor of Engineering in 1986 from Bhopal University, Bhopal. He is currently AP at the Department of Electrical Engg., MANIT, Bhopal, India. His current research interest include power conditioning unit for Renewable Energy storage system particularly Solar Energy, Hybrid Energy Systems, Grid Interconnection of Renewable Energy sources and FACTS devices.

E-mail: rk_nema@yahoo.com

Kaushal K. Sao has received his M. Tech. degree in Heavy Electrical Equipment from MANIT, Bhopal in 2005. Currently he is working as Asstt. Manager at Emerson Network Power (I) Ltd., Thane (W), Mumbai, India. His field of interests are Power Converters and Drives.

E-mail: kkishoresao@yahoo.co.in

Paper No. 145-A;