A Series Connected Three-Level Inverter Topology For Medium Voltage Squirrel Cage Motor Drive Applications

Suvajit Mukherjee
Electrical Engineering Department
Indian Institute of Technology
Kharagpur, India
m_suvajit@yahoo.com

Gautam Poddar
Electrical Engineering Department
Indian Institute of Technology
Kharagpur, India
gpoddar@ee.iitkgp.ernet.in

***Abstract*— The application of PWM voltages using two level high voltage inverters to a squirrel cage induction motor (SQIM) can cause high bearing currents, heating of rotor shaft, voltage spike across the motor terminals, etc. The increase in the number of steps of the motor voltage and hence decreasing the *dv/dt* applied to the machine terminals can be a solution to this problem. The existing topologies that generate this multi-step voltage include cascading of a number of single-phase inverters or use of higher order multi-level inverters. In this paper a topology with series connection of three phase three-level inverters is proposed that addresses the problems of medium voltage drives. The design of the inverter topology and its various PWM techniques are presented in the paper. This inverter topology and its control are verified on a 7.5 hp squirrel cage induction motor (SQIM) drive. Experimental results validate the steady-state and dynamic performances of the drive.**

Keywords- Medium voltage ac drives, Multi-level converter topologies

NOMENCLATURE

L_s , L_r	Stator and rotor self inductances referred to the stator
L_0	Magnetizing inductance
σ_s , σ_r	Stator and rotor leakage factors
σ	Total leakage factor
R_s , R_r	Stator and rotor resistances referred to stator
P	Number of poles of the motor
V_{sd} , V_{sq}	d-axis and q-axis stator voltages
V_{rd} , V_{rq}	d-axis and q-axis rotor voltages
ε	Angle between stator and rotor axes
ρ_{mr} , ρ_r	Rotor flux angle with respect to stator and rotor axis
$\vec{\psi}_{rs\alpha}$, $\vec{\psi}_{rs\beta}$	α-β axis rotor flux in stationary reference frame

I. INTRODUCTION

In normal squirrel cage induction motor (SQIM) drive, the motor normally is fed with pulse width modulated (PWM) voltages which cause high bearing currents (due to *dv/dt*) and heating of rotor shaft [1, 14]. In certain applications, shaft voltages [1] can cause direct damage, e.g., sparks in a hazardous environment, and are very undesirable. This is a matter of big concern for variable speed medium voltage drives where the voltage levels are very high. The above problem can be resolved by applying variable voltage with low *dv/dt*. By increasing the number of steps of the motor voltage like multi-cell technologies [2, 3], the gravity of this problem can be reduced. The proposed topology of series connected three-level inverters increases the number of steps in the applied voltage and hence decreasing the *dv/dt* applied to the machine terminals.

Similar voltage profiles can also be obtained by using higher order neutral point clamped (NPC) multi-level inverters [4, 5] or by cascading a number of two level inverters [2, 3]. But, the multi-level NPC inverters suffer from dc bus imbalance [11-13], device underutilization problems and unequal ratings of the clamped diodes, etc [5, 6] which are not so serious problems for the inverters with three-level or below. The capacitor voltage imbalance for five-level are presented in [11-13] which suggest the need of extra hardware in the form of dc choppers or a back to back connection of multilevel converters. The cascaded H-bridge topology [2-4] suffers from the drawbacks of usage of huge dc bus capacitors and complex input transformers for isolated dc bus for each module. These drawbacks are addressed in the proposed topology. Furthermore, the power circuit is modular in structure and hence the number of modules to be connected in series depends on the power of the drive.

In this paper, the proposed topology and its various PWM control strategies are experimentally validated on a vector controlled squirrel cage induction motor drive [8-10]. It has two three-level inverters connected in series and drives the motor.

II. POWER CONVERTER TOPOLOGY

The proposed general configuration of *'n'* number of three-level inverters connected in series is shown in figure 1. Each inverter module is a three-phase neutral point clamped (NPC) three-level inverter. At the output stage, transformers are used to have the series connection of three-level inverters as shown in figure 1. If 'V_{dc}' is the dc bus voltage of each inverter module, 'α' is the turns ratio of each transformer, and '*n*' is the

number of inverter modules then for sine PWM strategy, the motor rms phase voltage (V_{Ph_motor}) can be expressed as follows.

$$\text{rms of } V_{Ph\_motor} = \sqrt{3}\alpha mn\frac{V_{dc}}{2\sqrt{2}} \quad (1)$$

where m is the modulation index of the inverter topology defined as follows.

$$m = \frac{peak\ of\ V_{ph\_inverter}}{n\frac{V_{dc}}{2}} \quad (2)$$

$V_{ph\_inverter}$ is the total phase voltage reference of the inverter topology. For given peak of V_{Ph_motor} , $peak\ of\ V_{ph\_inverter}$ can be computed as below.

$$peak\ of\ V_{ph\_inverter} = \frac{peak\ of\ V_{ph\_motor}}{\sqrt{3}\alpha} \quad (3)$$

The generation of individual reference voltage signal of each inverter is discussed as follows.

The gate pulses for each three-level inverter module can be derived using two carrier signals. Thus, '*n*' numbers of such three-level inverter modules require '*2n*' number of carriers [6, 7]. The three-phase voltage reference signals are then compared with these carrier waves to produce the gate pulses for the inverters. For example, the carrier waves and the sinusoidal modulating voltage signal (SPWM technique) for R-phase is shown in figure 2 for 4 numbers of series connected three-level inverters. The carrier waves 1 and 1/ (figure 2) with R-phase voltage reference controls the inverter module 1. Similarly, 2-2/, 3-3/, and 4-4/ carrier waves with R-phase voltage reference generate the gate pulses for the three-level inverter modules 2, 3, and 4 respectively. Thus each inverter module produces the voltage proportional to a part of the reference phase voltage signals. It is important to note that no two three-level inverter modules switch simultaneously (figure 2). Thus, the maximum *dv/dt* rate of the output voltage of this topology is limited to that of a single three-level inverter module (figure 5). The references of each inverter are shown in figure 3. The corresponding output line voltages of each inverter are shown in figure 4. The four windings, one from each transformer, are connected in series and produced the net R-phase voltage as shown in figure 5. Similarly, the other two phase voltages are generated.

The line voltage spectrums of individual inverters are presented in figure 4 for switching frequency of 2.5 kHz. These line voltages get added to produce the net phase voltage of the topology. The voltage spectrums are expressed as a percentage of the maximum total fundamental (V_{peak}) that can be produced by the topology.

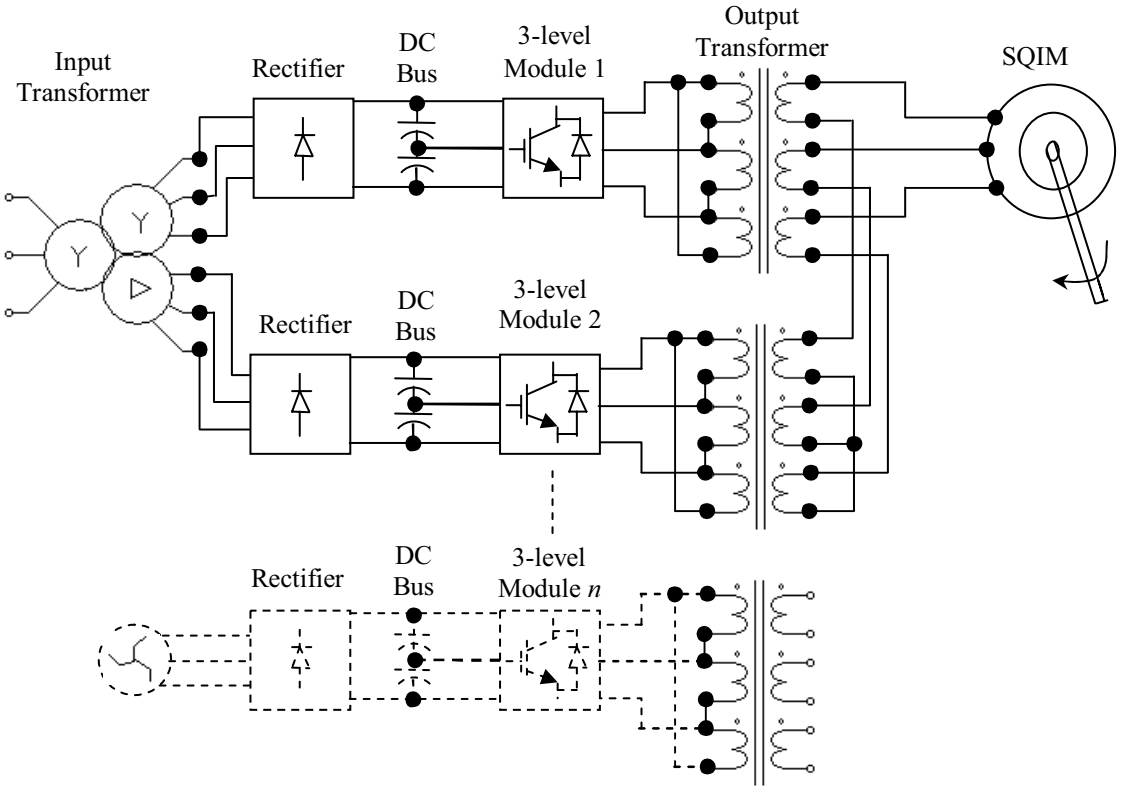


Fig.1. Block diagram of three phase three-level inverter modules connected in series driving a SQIM

$$V_{peak} = \sqrt{2} * V_{Ph\_motor} \quad (4)$$

or, $V_{peak} = 2078.5\ V$ for $V_{dc} = 600$ V, $n = 4$, $\alpha = 1$ and $m = 1$ using equation (1). Hence the spectrums show the percentage share of the fundamental of each inverter module. These spectrums also suggest that the line voltages of all these inverters contain additional small amount of 5th, 7th, 11th, 13th, and higher order harmonics besides the normal switching harmonics. However, the net phase voltage and line voltage of this topology do not contain any of these harmonics as suggested by the spectrums shown in figure 5. These harmonics get canceled when the line voltages of the individual inverters are added by the transformers to produce the net phase voltages.

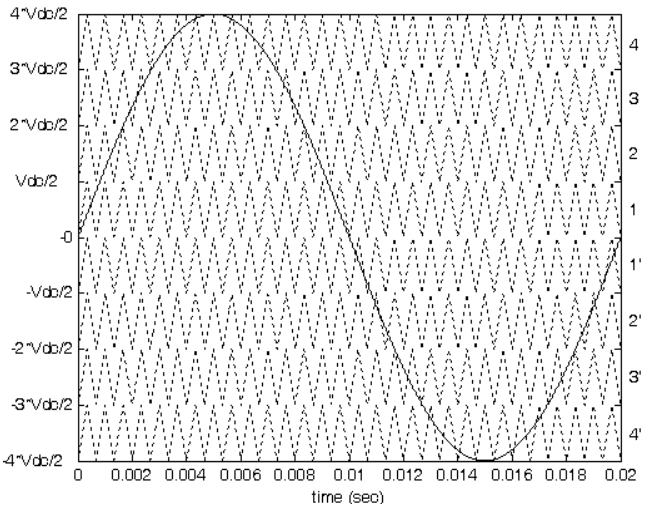


Fig.2. The carrier waves and the sinusoidal modulating voltage signal for R-phase in sine PWM (SPWM) technique

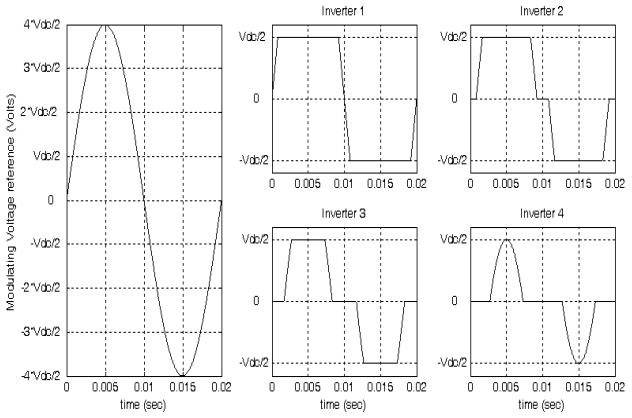


Fig.3. Generation of modulating voltage signal for R-phase of each of the four inverters in series for sine PWM strategy

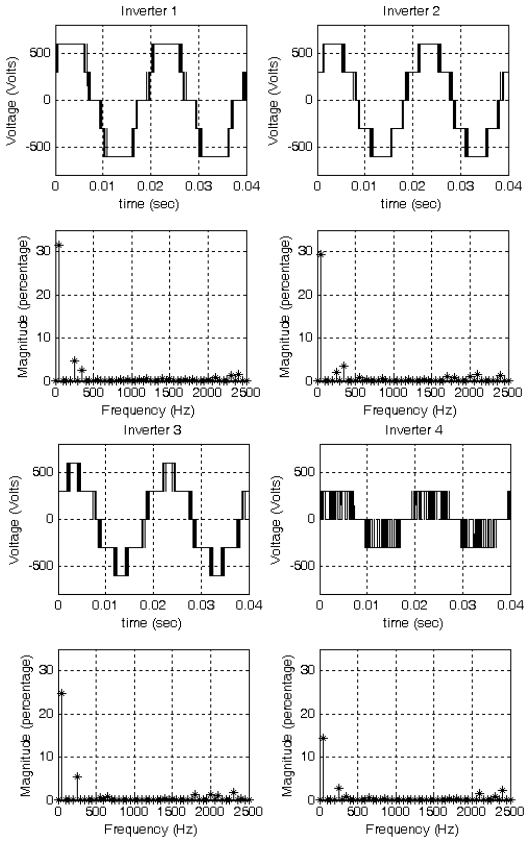


Fig.4. Simulated line voltage and harmonic spectrum of inverter 1, inverter 2, inverter 3 and inverter 4 when four inverters are connected in series with sine PWM technique for $V_{dc} = 600$V, $\alpha = 1$ and $m = 1$

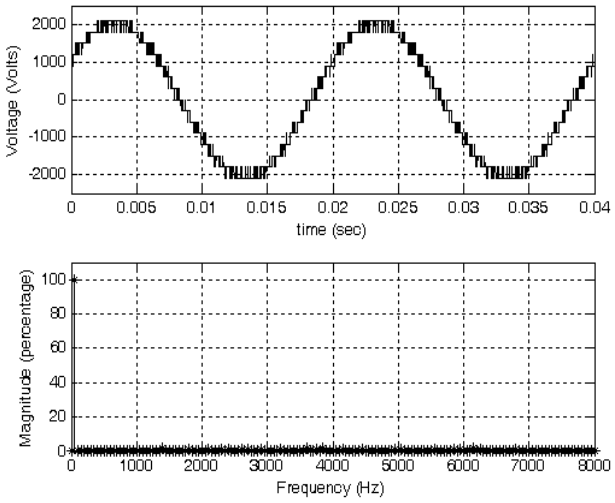


Fig.5. Simulated phase voltage when four inverters are connected in series with sine PWM technique for $f_{sw} = 2.5$ kHz, $V_{dc} = 600$ V, $\alpha = 1$ and $m = 1$

III. Design Of Inverter Modules

The general configuration of a sensorless squirrel cage induction motor drive with *'n'* number of 3-phase voltage source modules connected in series is shown in figure 1. Each voltage source module consists of a three-phase diode rectifier, a dc bus, a three-phase three-level NPC inverter and a three-phase transformer. In this section, design guidelines are presented for each module to drive a motor of voltage and current ratings V_s and I_s respectively.

A. Design of transformer and inverter for each module

The primary side of each 3-phase transformer is chosen as delta connected while the secondary side is kept open for the series connection between the modules. Normally, the dc bus voltage (V_{dc}) of each module is chosen such that the standard IGBT module (say, 1400V IGBT, 300A) can be used. Similarly, the current rating (I_{inv}) of each inverter module is chosen. Now, the current required on the motor side of the transformer is I_s. Then the current drawn from the inverter is $I_s * \alpha * \sqrt{3}$ and must be equal to I_{inv}. Here, α is the transformer turns ratio defined as follows.

$$\alpha = \frac{number\ of\ transformer\ phase\ turns\ on\ the\ motor\ side}{number\ of\ transformer\ phase\ turns\ on\ the\ inverter\ side} \tag{5}$$

Thus, the turns ratio of the transformer (α) is obtained as below.

$$\alpha = \frac{I_{inv}}{\sqrt{3} * I_s} \tag{6}$$

For n number of modules, the maximum line voltage, this topology can produce, is $\sqrt{3} * V_{dc} \frac{\alpha * n}{\sqrt{2}}$ assuming space vector PWM strategy. This voltage must match the required motor line voltage V_s. Thus, the number of modules n can be selected as below.

$$n = \frac{\sqrt{2} * V_s}{\sqrt{3} * \alpha * V_{dc}} = \frac{\sqrt{2} * V_s * I_s}{V_{dc} * I_{inv}} \tag{7}$$

At maximum modulation index in the linear modulation zone, all the modules share the net fundamental output voltages almost equally. Additionally, all the modules also have some amount of 5th, 7th, and higher order voltage harmonics besides very small amount of switching harmonics. These voltage harmonics must be taken care of while designing the standard transformer for each module. However, all the module currents and hence the transformer currents remain almost sinusoidal.

B. Selection of DC Bus Capacitor for Each Module

In single phase inverters the dc bus carries second harmonic currents in addition to the switching currents. So the size of the capacitors increases when single phase inverters are used in cascaded H-bridge topology [2]. Since the proposed drive has three-phase inverter at the output stage the low frequency (second harmonic) ripple in the capacitor will not be present. So, the size of the capacitor will be relatively small in the case of the proposed topology.

IV. SQIM Drive Using Proposed Converter

The general configuration of a sensorless squirrel cage induction motor drive with *'n'* number of neutral point clamped (NPC) three-level inverter is shown in figure 1. All the three-level inverters, connected in series, drive the motor and share the load.

A. Rotor-Flux Oriented Squirrel Cage Induction Motor

In this topology the stator leakage inductance value has to be modified to incorporate the leakage inductance of the output transformers (L_{lT}). Also the effective stator resistance changes due to the presence of transformer winding resistances (R_{lT}). By neglecting the magnetizing branch of the inverter transformer, the equivalent circuit of the transformer is a simple *R-L* circuit as shown in figure 6. Thus the modified values of the stator leakages are as follows.

$$\begin{aligned} \sigma L_s^{/} &= \sigma L_s + L_{lT} \\ R_s^{/} &= R_s + R_{lT} \end{aligned} \tag{8}$$

Hence the modified dynamical equations of the SQIM voltages and currents in d-q plane are presented as follows.

$$V_{sd} = R_s^{/} i_{sd} + \sigma L_s^{/} \frac{di_{sd}}{dt} - \underline{\sigma L_s^{/} \omega_{mr} i_{sq}} + \underline{\frac{1}{(1+\sigma_r)} \frac{d\psi_r}{dt}} \tag{9}$$

$$V_{sq} = R_s^{/} i_{sq} + \sigma L_s^{/} \frac{di_{sq}}{dt} + \underline{\sigma L_s^{/} \omega_{mr} i_{sd}} + \underline{\frac{\psi_r \omega_{mr}}{(1+\sigma_r)}} \tag{10}$$

Here, the d-axis is aligned with the rotor flux vector ($\vec{\psi}_r$) [10, 16]. The rotor flux vector in stationary coordinates ($\vec{\psi}_{rs}$) is expressed in terms of stator flux as

$$\vec{\psi}_{rs} = \frac{L_r}{L_0} \{\vec{\psi}_s - \sigma L_s \vec{i}_s\} \tag{11}$$

The stator flux $\vec{\psi}_s$ is estimated from stator voltage $\vec{V}_s$ as below.

$$\vec{\psi}_s = \int (\vec{V}_s - R_s \vec{i}_s - \omega_c \vec{\psi}_s) \tag{12}$$

The problem integration at low frequency is tackled by replacing the pure integration of stator voltage with a low-pass filter (cut-off frequency = ω_c) [10, 15].

B. Motor Controller

The d-axis and the q-axis motor voltage equations (9) and (10) show the first-order dynamics of the stator currents (i_{sd} and i_{sq}) if the underlined terms are decoupled. So, simple PI-controllers with unity feedback system can control the d-q axis motor currents to control the flux and the torque of the motor as shown in figure 7. By choosing the proper gain values of the PI controllers, the desired

bandwidth ($1/\tau_{im}$) of the motor current controller is achieved [10]. Thus, the closed loop transfer functions of i_{sd} and i_{sq} become as follows.

$$\frac{i_{sd}(s)}{i_{sd}^{*}(s)} = \frac{1}{1+s\tau_{im}} \quad and \quad \frac{i_{sq}(s)}{i_{sq}^{*}(s)} = \frac{1}{1+s\tau_{im}} \tag{13}$$

In the present work, the desired response time τ_{im} of the motor current is chosen as 4 msec. Finally, the outputs of the PI controllers are added to the underlined coupling terms of (9) and (10) to get the actual d-axis and the q-axis voltage references (V_{sd}^{*}, V_{sq}^{*}) [10].

It is important to note that the motor phase voltages and the inverter phase voltages are not in phase. The motor phase voltage is in phase with the line voltages of the inverter modules. Hence a phase shift of 30^{o} is provided to the three motor phase voltage references obtained to generate the three inverter phase voltage references. The phase reference obtained is the total phase reference of the topology. Hence this reference is obtained by adding the reference of the individual inverter modules.

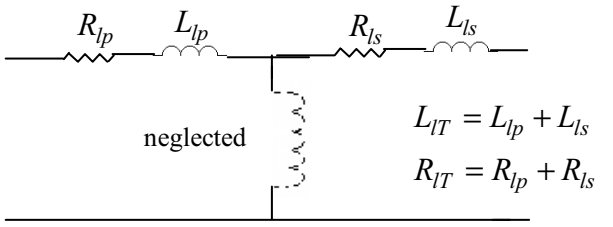


Fig.6. Equivalent circuit of a single phase transformer with 1:1 turns ratio

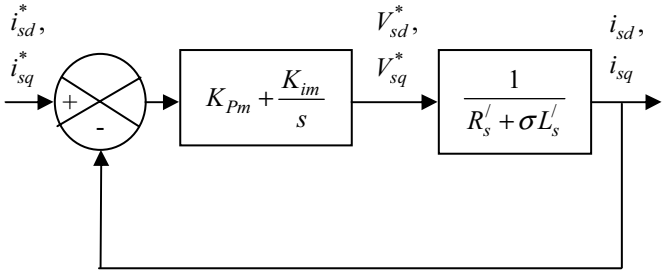


Fig.7. d-axis and q-axis motor current controller

V. EXPERIMENTAL RESULTS

The experimental verification is carried out on a 7.5-hp squirrel-cage induction motor. The inverters used for this drive are three-phase 5 KVA three-level diode clamped inverters. Two inverters are used to demonstrate the control strategy as discussed above. The switching frequency of the individual inverter is 5 kHz. The complete control strategy is implemented on a digital controller.

Figures 8 and 9 show the individual inverter line voltages that are being added up. The voltage references for individual converters in bus clamp technique are shown in figure 10. Figure 11 shows the inverter phase voltage references with carrier based PWM with third harmonic injection technique and also with centered space vector PWM technique [7]. The phase voltage waveform along with its spectrum analysis is shown in figure 12. It confirms stepped voltage waveform and low *dv/dt* that is applied to the motor. Figure 13 shows the steady state motor line voltage and motor current. Figure 14 shows the variation of motor phase voltage and motor speed for a step change in torque command. Figure 15 shows the response of the torque current (i_{sq}) for a step change in torque current command (i_{sq}^{*}). This figure suggests that the i_{sq} has a response time constant 4 ms as per designing.

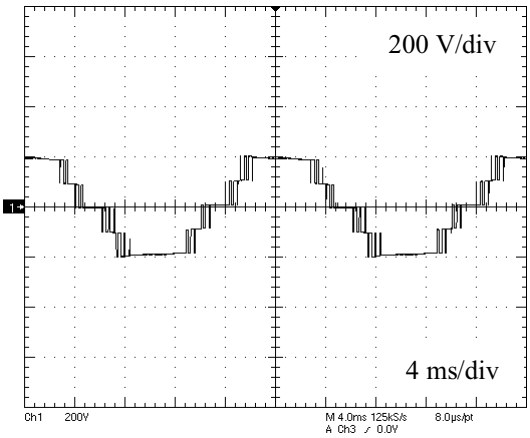


Fig.8. Experimental waveform of steady state inverter1 line voltage

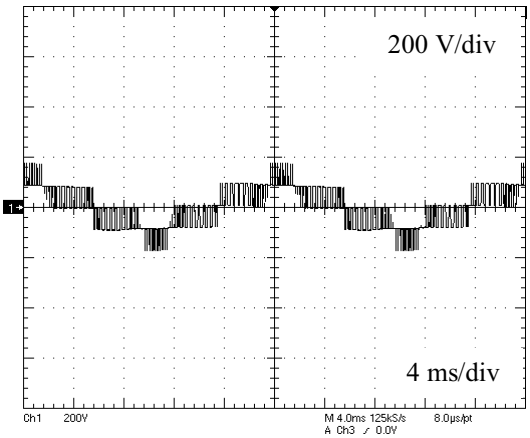


Fig.9. Experimental waveform of steady state inverter 2 line voltage

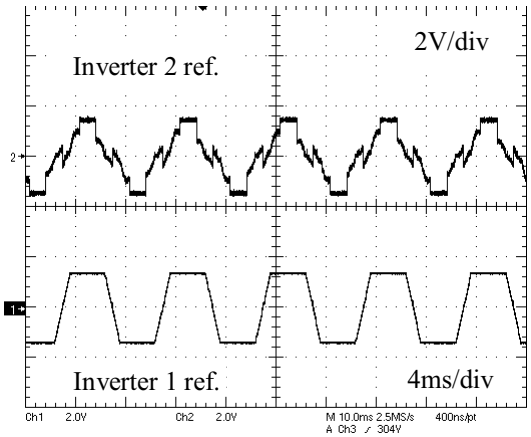
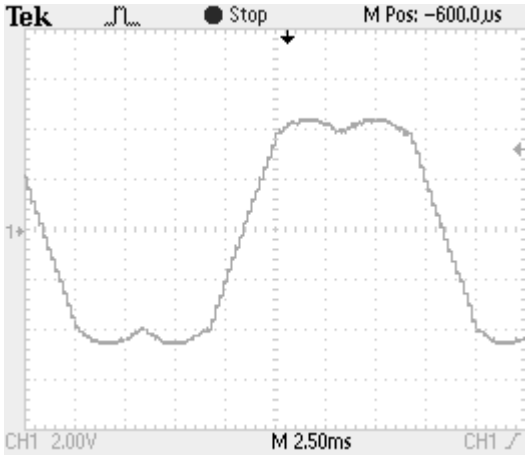
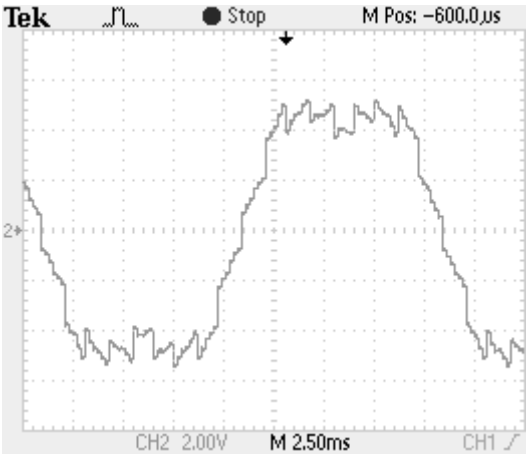


Fig.10. Experimental waveform of inverter references in bus clamp technique



(a)



(b)

Fig.11. Experimental waveform of inverter reference with (a) carrier based PWM with third harmonic injection technique; (b) centered space vector PWM technique

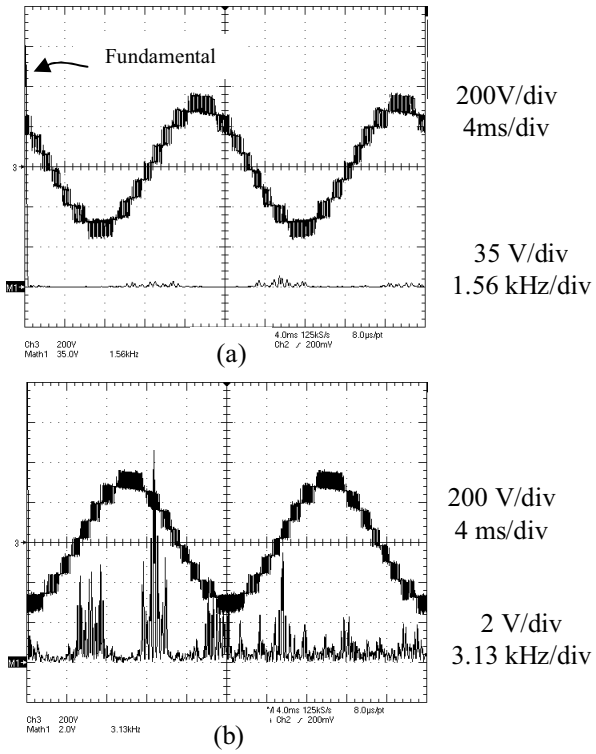


Fig.12. (a) Experimental waveform of steady state motor phase voltage (V_{s1}) and its spectral analysis showing the relative magnitude of fundamental and harmonics; (b) Zoomed harmonic spectrum (f_{sw} = 5 kHz)

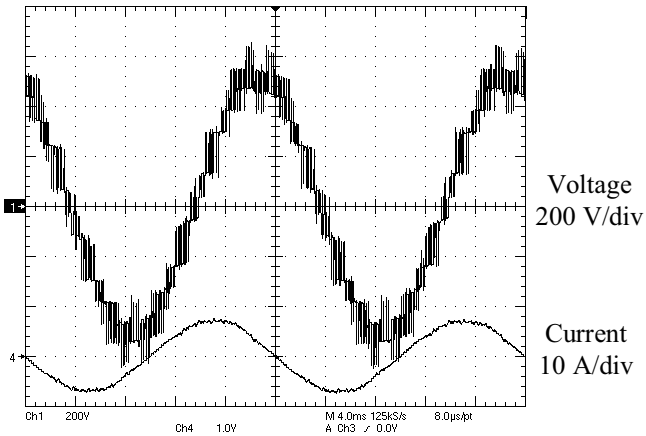


Fig.13. Experimental waveform of steady state motor current (i_{s1}) and motor line voltage

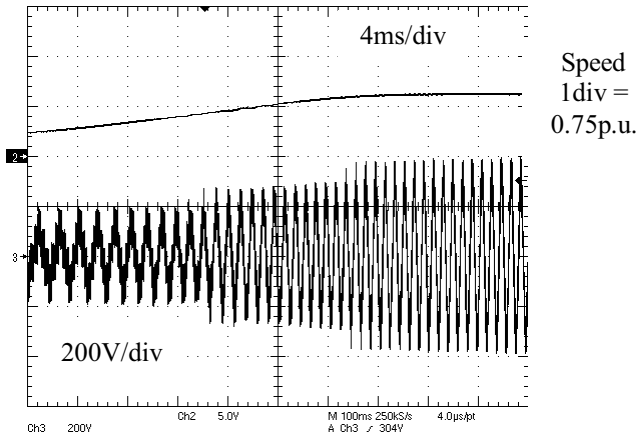


Fig.14. Motor phase voltage during speed transient

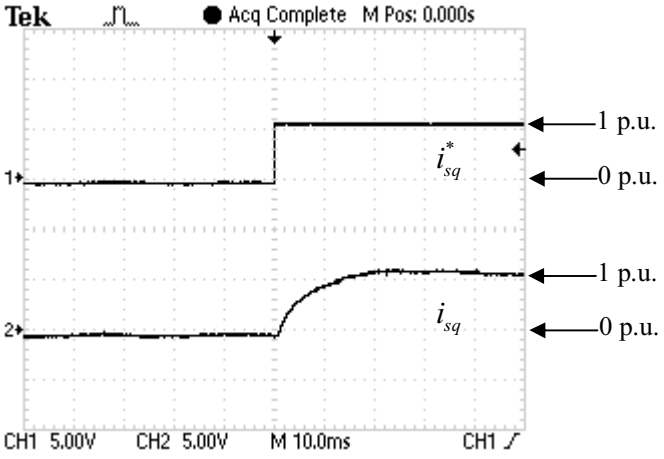


Fig.15. Torque current (i_{sq}) for step change in torque current command (i_{sq}^*)

VI. CONCLUSION

A series connection of three-level inverters is proposed for medium voltage sensorless vector control SQIM drive with increased voltage capacity. The topology ensures high power operations with medium voltage output having several voltage levels. The reduction in the ratings of dc bus capacitor and reduced imbalance problems in the dc bus [11-13] are some of the advantages of the proposed topology over the existing topologies. The disadvantage of the proposed topology is that it requires additional output transformers which introduce additional cost and losses. However, these transformers do not have complex underutilized windings like that required in cascaded H-bridge topologies [2-4].

A scaled down (10 kVA) laboratory proto-model of this inverter is developed for vector controlled SQIM drive application. The topology is tested for SQIM drive application in the frequency range near 8Hz to 50Hz due to the problems of sensorless control in low frequency operations and also due to the problems of low frequency operation of a standard transformer.

Different PWM strategies are used for this inverter control. Using the feed forward control strategy for the motor, a first order response is achieved for the motor currents with a time constant of 4 msec. The motor terminal voltage shows a number of steps at different operating conditions. So, the life of the motor is also expected to be very high due to the low applied *dv/dt*. The modularity of the proposed drive gives flexibility in different high power applications. If one module of the topology fails, the inverter can operate at reduced power level similar to the single phase H-bridge topology [2].

APPENDIX

Motor Parameters:
Rated power 7.5 hp;
Rated frequency 50Hz;
Rated speed 1435rpm;
Number of pole 4;
Stator line voltage 415V;
Rated line current 10.8A;
$R_s = 1.3\Omega$; $R_r = 0.476\Omega$;
$L_0 = 0.1310H$; $\sigma_s = 0.0396H$; $\sigma_r = 0.0396H$;

REFERENCES

[1] Fei Wang, "Motor Shaft Voltages and Bearing Currents and their Reduction in Multilevel Medium-Voltage PWM Voltage-Source-Inverter Drive Applications," *IEEE Transactions on Industry Applications*, Vol.36, No. 5, September/October 2000, pp. 1336-1341.

[2] P.W. Hammond, "A New Approach to Enhanced Power Quality for Medium Voltage Drives", *IEEE Transactions on Industry Applications*, Vol.33, No.1, January/February 1997, pp.202-208.

[3] R. Teodorescu, F. Blaabjerg, J.K. Pederson, E. Cengelci, P.N. Enjeti, "Multilevel Inverter by Cascading Industrial VSI", *IEEE Trans. on Industrial Electronics*, vol.49, no. 4, pp. 832-838 August 2002.

[4] Akira Nabae, Isao Takahashi and Hirofumi Akagi, "A new neutral point clamped inverter", *IEEE Trans. on Industry Applications*, vol.17, no.5, Sept/Oct.1981, pp. 518-523.

[5] Jih-Sheng Lai and Fang Zheng Peng, "Multilevel converters - a new breed of power converters," *IEEE Transactions on Industry Applications*, Vol. 32, No. 3, pp. 509–517, May/June 1996.

[6] G. Cararra, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A

theoretical analysis," *IEEE Transactions on Power Electronics*, Vol.7, No.3, July 1992, pp. 497-505.

[7] B.P.McGrath, D.G.Holmes and T.A.Lipo, "Optimized space vector switching sequences for multilevel inverters", *IEEE Transaction Power Electronics*, vol.18, no.6, Nov. 2003, pp 1293 - 1301.

[8] K. D. Hurst, T. G. Habetler, G. Griva, and F. Profumo, "Zero-speed tacholess IM torque control: simply a matter of stator voltage integration," *IEEE Transactions on Industry Applications*, Vol.34, No.4, pp. 790–795, July/Aug. 1998.

[9] T. Ohtani, N. Takada, K. Tanaka, "Vector Control of Induction Motor without Shaft Encoder," *IEEE Trans. Industry Applications*, vol.28, no.1, Jan/Feb 1992.

[10] Suvajit Mukherjee and Gautam Poddar, "Fast Control of Filter for Sensorless Vector Control SQIM Drive with Sinusoidal Motor Voltage", *IEEE Transactions on Industrial Electronics*, Vol. 54, No. 5, October 2007.

[11] Newton, C., and Summer, M., 'Novel technique for maintaining balanced internal DC-link voltages in diode-clamped five-level inverters', IEE Proc. EPA, 1999, 146, (3), pp. 341–349

[12] Choi, N.S., Cho, J.G., and Cho, G.H., 'A general circuit topology of multilevel inverter'. Proc. of 22nd Annual IEEE Conf., ESC'91, 24–27 June 1991, pp. 96–103

[13] Marchesoni, M., and Tenca, P., 'Diode-clamped multilevel converters: a practicable way to balance DC-link voltages' *IEEE Transactions on Industrial Electronics*, 2002, Vol.49, No.4, pp. 752–765.

[14] Muetze, A. and Binder, A, 'Calculation of Circulating Bearing Currents in Machines of Inverter-Based Drive Systems' *IEEE Transactions on Industrial Electronics*, 2007, Vol.54, No.2, pp. 932–938.

[15] K. D. Hurst, T. G. Habetler, G. Griva, and F. Profumo, "Zero-speed tacholess IM torque control: simply a matter of stator voltage integration," *IEEE Transactions on Industry Applications*, Vol.34, No.4, pp. 790–795, July/Aug. 1998.

[16] W. Leonhard, "Control of Electrical Drives", Springer-Verlag, 1985.