Space Vector Pulse Width Modulation Applied to the Three-Level Voltage Inverter

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***Abstract*—Advances in power electronics technology allowed the wide investigation of multilevel converters that provide high safety voltages with less harmonic components compared to the two-level structures. Employed for converter's gating signals generation, the space-vector pulse width modulation (SVPWM) strategy reduces the switching losses by limiting the switching to the two thirds of the pulse duty cycle.**
This study aims to explain, via simple and easy algebraic expressions, the application of the SVPWM on the three-level voltage inverter. The theoretical study was numerically simulated using Simulink under Matlab software.

***Index Terms*—Three-level voltage inverter, space vector pulse width modulation, DC-link voltage, sampling time.**

I. INTRODUCTION

Multilevel converters structures, in their two configurations cascaded and neutral-point clamped (NPC), are well-known since 20 years ago [1].They were investigated with the requirement of quality and efficiency in a high power systems. The fame of these lasts is due to many advantages that they offer: increased power rating, improved harmonic performance and reduced electromagnetic interference (EMI) emission [2]. In fact, the main switching devices have to block only one-half of the DC-bus voltage, also, there is less harmonic content in the multilevel converters voltages spectrums compared with the standard two level ones [3]. The most common configuration of multilevel converters is the neutral point clamped voltage source inverter structure (VSI-NPC) which is widely used in medium voltage drives for rolling mills, marine, and traction applications [4]. The cascaded topology is generally employed in voltage industrial drives, electric vehicles, and grid connection of photovoltaic cell generation systems [2].

To control multilevel converters, the pulse width modulation (PWM) strategies are the most effective, especially the space vector pulse width modulation (SVPWM) one, which has equally divided zero voltage vectors describing a lower total harmonic distortion (THD) [5]. Although the complexity that presents the SVPWM strategy (many output vectors) compared with the carrier-based PWM one, it remains the preferred seen that it reduces the power losses by minimizing the power electronic devices switching frequency (limiting the minimum pulse width) [5], [6].

In this paper, a theoretical study and computer simulation works of the three-level voltage inverter with NPC structure controlled with the space vector modulation SVPWM strategy is presented. This study is based on simple algebraic equations linking the pulses of the gating to the phase reference voltages.

II. SYSTEM DESCRIPTION, FUNCTIONING, MODELING, AND THEORETICAL SIGNALS

A. Description

As shown on Fig. 1, the studied system is constituted of a DC supply, and a three-level voltage inverter bridge based on MOSFET's/Diodes pairs. Each arm contains four MOSFETs, four antiparallel diodes and two neutral clamping diodes. The inverter is feeding an AC load through a three-phase transformer.

B. Functioning

The three-level voltage inverter outputs three-level voltages (-E/2, 0, E/2) depending on the DC-bus voltage *E* and the variable state *Ci*, where '*i*' is the phase indicator (*i* = a, b, c) [6],[7]. Si_1, Si_2, Si_2', Si_1' are the switches of one leg, and V_{io} is the phase-to-fictive middle point voltage. The functioning principle is displayed on Table 1. In order to obtain the desired three-level voltages, the converter must ensure complementarities between the pairs of switches: (Si_1,Si_2') and (Si_2,Si_1').

C. Modeling

For modeling, we follow the steps described in [7] and [8].

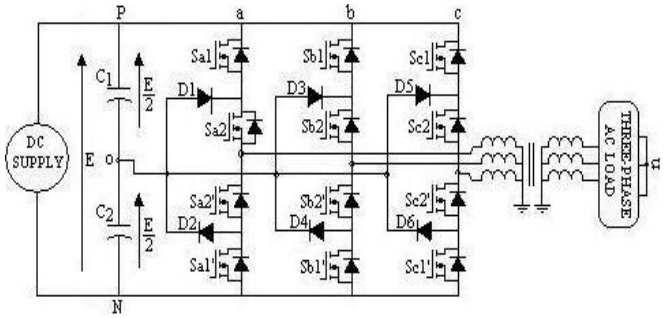


Fig. 1. Studied system description.

TABLE 1
THREE-LEVEL INVERTER FUNCTIONING'S PRINCIPLE.

Ci	Si_1	Si_2	Si_2'	Si_1'	V_{io}
1	1	1	0	0	$E/2$
0	0	1	1	0	0
-1	0	0	1	1	$-E/2$

V_{io} is linked to E through (1):

$$Vio = Ci \,.\, E / 2 \tag{1}$$

The phase-to-neutral point voltage V_{in} depends on V_{io} via (2), ($i = a, b, c$):

$$V_{in} = V_{io} - V_{no} \tag{2}$$

Assuming that the system is balanced, the sum of V_{in} is equal to zero:

$$V_{an} + V_{bn} + V_{cn} = 0 \tag{3}$$

Then, (2) and (3) end at:

$$V_{no} = 1/3 \,.\, (V_{ao} + V_{bo} + V_{co}) \tag{4}$$

By replacing V_{no} in (2), we obtain the following system:

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} . \begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} \tag{5}$$

Let now apply the Concordia transformation to the vector V_{in} giving it in the diphase (α-β) frame:

$$\begin{bmatrix} V_{\alpha} \\ V_{\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} . \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} . \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{6}$$

Now, considering the 'm' states (m = 1, 0, -1) of the variable Ci, we obtain the 'm^q' possible combination of the three-level voltage inverter ('q' is the phase number, here q = 3). The result is 27 vectors grouped in Table 2, where we notice that there are 03 zero vectors (V_0, V_7, V_{14}), and a group of 12 vectors representing in pairs the same coordinates (α-β): (V_{11},V_{12}) , (V_{21},V_{22}), (V_{31},V_{32}), (V_{41},V_{42}), (V_{51},V_{52}), and (V_{61},V_{62}). By drawing these 27 vectors in the (α-β) frame, as illustrated on Fig. 2, we can distinguish between the three hexagons displayed on Fig. 3:

- *The small hexagon* (Fig.3.a), defined by the six regions I, II, III, IV, V, and VI. All vectors limiting these regions have the same magnitude: $E/\sqrt{6}$.
- *The middle hexagon* (Fig.3.b), defined by the six regions a, b, c, d, e, and f. All vectors limiting these regions have the

TABLE 2
THE 27TH THREE-LEVEL THREE-PHASE VOLTAGE INVERTER'S OUTPUTS.

Ca	Cb	Cc	Sa1	Sa2	Sb1	Sb2	Sc1	Sc2	Vao	Vbo	Vco	Van	Vbn	Vcn	Vα	Vβ	Vinv	N°
0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	V0	1
1	0	0	1	1	0	1	0	1	E/2	0	0	E/3	-E/6	-E/6	E/√6	0	V11	2
0	-1	-1	0	1	0	0	0	0	0	-E/2	-E/2	E/3	-E/6	-E/6	E/√6	0	V12	3
1	1	0	1	1	1	1	0	1	E/2	E/2	0	E/6	E/6	-E/3	E/√24	E/√8	V21	4
0	0	-1	0	1	0	1	0	0	0	0	-E/2	E/6	E/6	-E/3	E/√24	E/√8	V22	5
0	1	0	0	1	1	1	0	1	0	E/2	0	-E/6	E/3	-E/6	-E/√24	E/√8	V31	6
-1	0	-1	0	0	0	1	0	0	-E/2	0	-E/2	-E/6	E/3	-E/6	-E/√24	E/√8	V32	7
0	1	1	0	1	1	1	1	1	0	E/2	E/2	-E/3	E/6	E/6	-E/√6	0	V41	8
-1	0	0	0	0	0	1	0	1	-E/2	0	0	-E/3	E/6	E/6	-E/√6	0	V42	9
0	0	1	0	1	0	1	1	1	0	0	E/2	-E/6	-E/6	E/3	-E/√24	-E/√8	V51	10
-1	-1	0	0	0	0	0	0	1	-E/2	-E/2	0	-E/6	-E/6	E/3	-E/√24	-E/√8	V52	11
1	0	1	1	1	0	1	1	1	E/2	0	E/2	E/6	-E/3	E/6	E/√24	-E/√8	V61	12
0	-1	0	0	1	0	0	0	1	0	-E/2	0	E/6	-E/3	E/6	E/√24	-E/√8	V62	13
1	1	1	1	1	1	1	1	1	E/2	E/2	E/2	0	0	0	0	0	V7	14
1	0	-1	1	1	0	1	0	0	E/2	0	-E/2	E/2	0	-E/2	E.√3/√8	E/√8	V8	15
0	1	-1	0	1	1	1	0	0	0	E/2	-E/2	0	E/2	-E/2	0	E/√2	V9	16
-1	1	0	0	0	1	1	0	1	-E/2	E/2	0	-E/2	E/2	0	-E.√3/√8	E/√8	V10	17
-1	0	1	0	0	0	1	1	1	-E/2	0	E/2	-E/2	0	E/2	-E.√3/√8	-E/√8	V11′	18
0	-1	1	0	1	0	0	1	1	0	-E/2	E/2	0	-E/2	E/2	0	-E/√2	V12′	19
1	-1	0	1	1	0	0	0	1	E/2	-E/2	0	E/2	-E/2	0	E.√3/√8	-E/√8	V13	20
-1	-1	-1	0	0	0	0	0	0	-E/2	-E/2	-E/2	0	0	0	0	0	V14	21
1	-1	-1	1	1	0	0	0	0	E/2	-E/2	-E/2	2. E/3	-E/3	-E/3	E.√2/√3	0	V15	22
1	1	-1	1	1	1	1	0	0	E/2	E/2	-E/2	E/3	E/3	-2.E/3	E/√6	E/√2	V16	23
-1	1	-1	0	0	1	1	0	0	-E/2	E/2	-E/2	-E/3	2. E/3	-E/3	-E/√6	E/√2	V17	24
-1	1	1	0	0	1	1	1	1	-E/2	E/2	E/2	-2.E/3	E/3	E/3	-E.√2/√3	0	V18	25
-1	-1	1	0	0	0	0	1	1	-E/2	-E/2	E/2	-E/3	-E/3	2.E/3	-E/√6	-E/√2	V19	26
1	-1	1	1	1	0	0	1	1	E/2	-E/2	E/2	E/3	-2.E/3	E/3	E/√6	-E/√2	V20	27

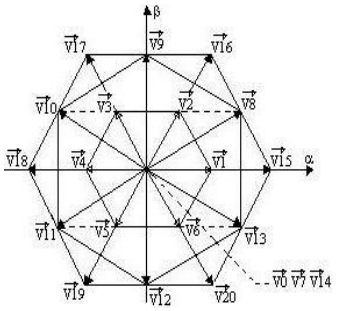


Fig. 2. Three-level voltage inverter vectors in the (α-β) frame.

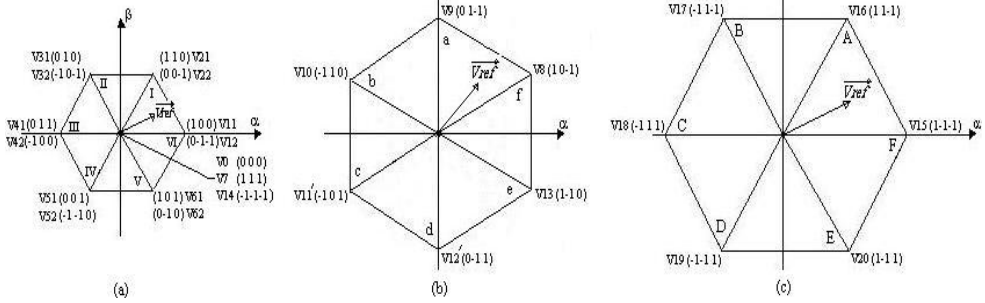


Fig.3. Three-level inverter's hexagons. (a). Small hexagon. (b). Middle hexagon. (c). Big hexagon.

same magnitude: $E/\sqrt{2}$.

- *The big hexagon* (Fig.3.c), defined by the six regions A, B, C, D, E, and F. All vectors limiting these regions have the same magnitude: $E.(\sqrt{2}/\sqrt{3})$.

D. Theoretical signals

According to [9], the theoretical signals that outputs the three-level voltage inverter, representing V_{io} and V_{in} respectively, are as displayed on Fig.4 (case of phase a). Here, we can see three voltage levels on V_{ao}: -E/2, 0, and E/2, and three voltage levels on V_{an}: E/3, E/2, and 2E/3.

III. INVERTER'S GATING SIGNALS GENERATION

Several strategies are proposed in order to generate the inverter's gates pulses. In this work, we used the space vector modulation SVPWM, which is a kind of the pulse width modulation PWM strategies [8], [10].

In this topic, the principle and the description of the SVPWM strategy will be detailed and applied to the three-level voltage inverter in an open loop functioning.

A. Principle

As shown on Fig. 3, in each of the three hexagons, the reference vector V_{ref} is located in one of the six regions constituting the hexagon, where each region is limited by two adjacent vectors V_δ et $V_{\delta+1}$ (Fig.5). Then V_{ref} is equal to:

$$\vec{V}_{ref} = \frac{T_\delta}{Ts}\vec{V}\delta + \frac{T_{\delta+1}}{Ts}\vec{V}_{\delta+1} \qquad (7)$$

Ts is the sampling time, T_δ, $T_{\delta+1}$ are the application times of V_δ and $V_{\delta+1}$ respectively. In one sample time, V_{ref} is equal to V_δ during T_δ and $V_{\delta+1}$ during $T_{\delta+1}$. In the rest of Ts, V_{ref} is equal to the zero vectors (V_{14}, V_0, and V_7) during T_0 following this optional choice: V_{14}, V_0 at the pulse's ends and V_7 at the pulse's centre.

At the same time:

$$\vec{V}_{ref} = \vec{V}_{ref\alpha} + \vec{V}_{ref\beta} \qquad (8)$$

Or, in complex writing:

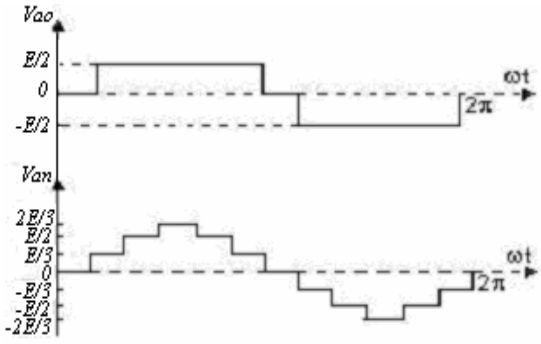


Fig. 4. Theoretical voltages of the three-level inverter.

$$\vec{V}_{ref} = \sqrt{V_{ref\alpha}^{\ 2} + V_{ref\beta}^{\ 2}}.e^{j(\varphi-\pi/2)} \qquad (9)$$

Where φ is an angle varying from 0 to 2π.

Then,

$$T_0 = T_S - T_\delta - T_{\delta+1} \qquad (10)$$

The SVPWM pulse is a pulse which is symmetrical and where all switches of the inverter's half-bridge have the same state in the centre and in the two ends. So, following these properties and after calculation of T_δ ,$T_{\delta+1}$ and T_0 of each region belonging to the appropriate hexagon, we arrive to build the pulses of the higher half-bridge (Si_1, Si_2, i = *a*, *b*, *c*, with Si_2', Si_1' as respective complementarities) of the three-level inverter.

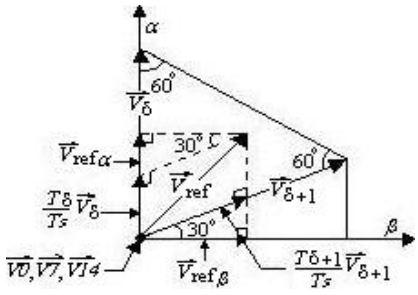


Fig. 5. Space vector modulation principle

B. Switching times calculation

As said previously, we distinguish between 03 hexagons (Fig. 3), where each one is constituted of 06 regions. As a result, we have 18 regions that wait the calculation of their respective switching times. To simplify this task, and for reason of similarities in the 06 regions of one hexagon on the one hand, and resemblance between hexagons 'a' and 'c' on the other hand (the largest magnitude in hexagon 'a' ($E/\sqrt{6}$) constitutes the half of the largest magnitude in hexagon 'c' ($E.\sqrt{2}/\sqrt{3}$)), for these all reasons, in the switching times calculation's procedure presentation, only two regions of hexagon 'a' and hexagon 'b', corresponding to the positive components of $V_{ref,}$ will be considered (Fig. 6). The other switching times will be then deduced from these four regions. Remind-we that the limiting vectors (V_1 to V_{20}) magnitudes will take the following values:

V_1 to $V_6 \rightarrow E/\sqrt{6}$, V_8 to $V_{13} \rightarrow E/\sqrt{2}$, V_{15} to $V_{20} \rightarrow E.(\sqrt{2}/\sqrt{3})$.
$V_7 = V_{14} = V0 = 0$.

- *Region I* (Fig.6.a) switching times calculation:

$$V_{ref\alpha} = (T_1 / T_S).V_1 + (T_2 / T_S).V_2.\sin(\pi/6) \quad (11)$$

$$V_{ref\beta} = (T_2 / T_S).V_2.\cos(\pi/6) \quad (12)$$

$$T_1 = \frac{\sqrt{6}Vref\alpha - \sqrt{2}Vref\beta}{E}.Ts \quad (13)$$

$$T_2 = \frac{2\sqrt{2}Vref\beta}{E}.Ts \quad (14)$$

- *Region II* (Fig.6.b) switching times calculation:

$$V_{ref\alpha} = ((T_2 / T_S).V_2 - (T_3 / T_S).V_3).\sin(\pi/6) \quad (15)$$

$$V_{ref\beta} = ((T_2 / T_S).V_2 + (T_3 / T_S).V_3).\cos(\pi/6) \quad (16)$$

$$T_2 = \frac{\sqrt{6}Vref\alpha + \sqrt{2}Vref\beta}{E}.Ts \quad (17)$$

$$T_3 = \frac{-\sqrt{6}Vref\alpha + \sqrt{2}Vref\beta}{E}.Ts \quad (18)$$

- *Region a* (Fig.6.c) switching times calculation:

$$V_{ref\alpha} = (T_8 / T_S).V_8.\cos(\pi/6) \quad (19)$$

$$V_{ref\beta} = (T_8 / T_S).V_8.\sin(\pi/6) + T_9 / T_S.V_9 \quad (20)$$

$$T_8 = \frac{2\sqrt{2}Vref\alpha}{\sqrt{3}E}.Ts \quad (21)$$

$$T_9 = \frac{\sqrt{6}Vref\beta - \sqrt{2}Vref\alpha}{\sqrt{3}E}.Ts \quad (22)$$

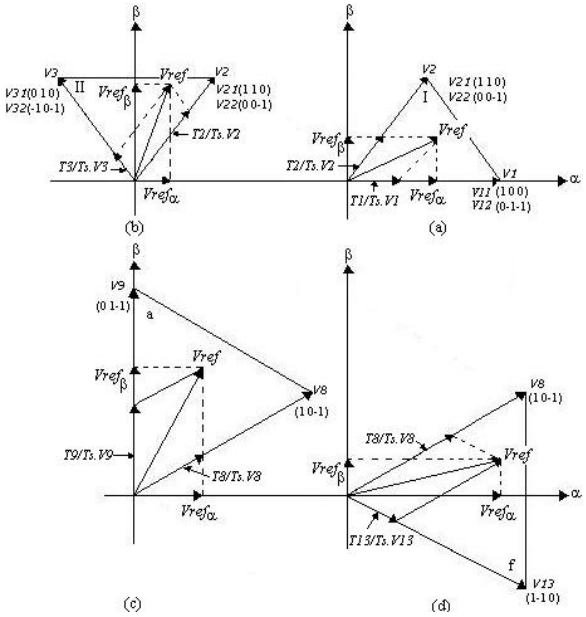


Fig. 6. Switching times calculation.

- *Region f* (Fig.6.d) switching times calculation:

$$V_{ref\alpha} = ((T_8 / T_S).V_8 + (T_{13} / T_S).V_{13}).\cos(\pi/6) \quad (23)$$

$$V_{ref\beta} = ((T_8 / T_S).V_8 - (T_{13} / T_S).V_{13}).\sin(\pi/6) \quad (24)$$

$$T_8 = \frac{\sqrt{6}Vref\beta + \sqrt{2}Vref\alpha}{\sqrt{3}E}.Ts \quad (25)$$

$$T_{13} = \frac{-\sqrt{6}Vref\beta + \sqrt{2}Vref\alpha}{\sqrt{3}E}.Ts \quad (26)$$

C. Examples of chronograms

Below are illustrated the pulses of regions 'I' and 'a' in Fig. 7.a and Fig.7.b respectively, where we can see a symmetrical signals that have the same states at the center and at the ends. Note that $T_{11} = T_{12} = T_1/2$, and $T_{21} = T_{22} = T_2/2$.
Then the zero voltage time application is given by:

$$T_0 = (T_S - T_\delta - T_{\delta+1})/6 \quad (27)$$

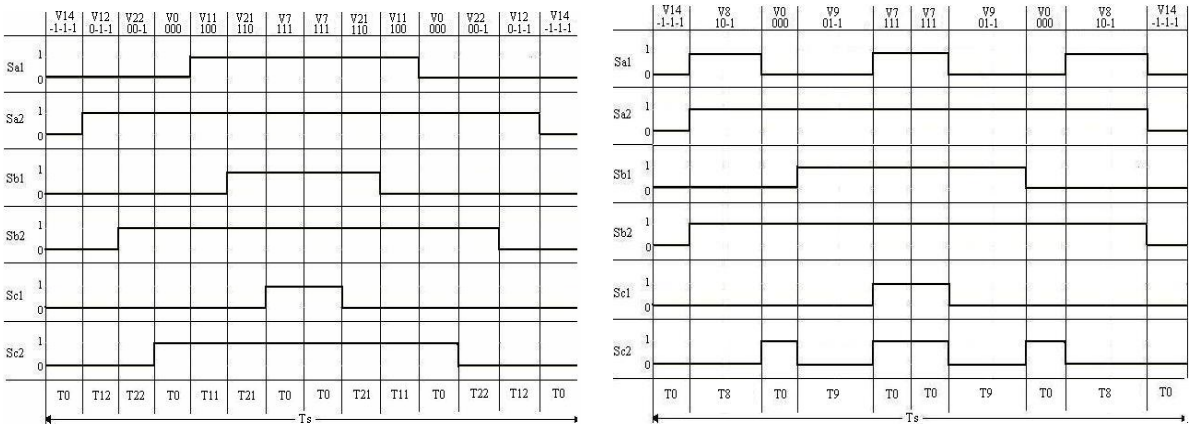
Where,

T_δ, $T_{\delta+1}$: times of V_δ and $V_{\delta+1}$.

D. Hexagons transition condition

The transition from a hexagon to the two others is function of the reference vector $V_{ref.}$ This last depends on the largest magnitude of each hexagon. We have:

- if ($-E/\sqrt{6} \le V_{ref} \le E/\sqrt{6}$) $\Rightarrow$ V_{ref} belongs to one of the six regions of the small hexagon 'a'.
- if ($-E/\sqrt{2} \le V_{ref} \le E/\sqrt{2}$) $\Rightarrow$ V_{ref} belongs to one of the six regions of the middle hexagon 'b'.
- if ($-E.\sqrt{2}/\sqrt{3} \le V_{ref} \le E.\sqrt{2}/\sqrt{3}$) $\Rightarrow$ V_{ref} belongs to one of the



(a) (b)

Fig. 7. Examples of chronograms. (a) Pulses of region I, small hexagon. (b). Pulses of region a, middle hexagon.

six regions of the big hexagon 'c'.

IV. Simulation studies

A. Simulation software

For simulation studies, we used Simulink under Matlab software. Especially, we employed S-functions blocs that allow the carrying out of linear programs in Simulink models.

B. Simulation considerations

For simulation of the above theoretical studies, we consider an open loop. As optionally choice, V_{ref} was determined by a system of balanced three-phase voltages given by (28).

$$\begin{aligned} ea &= Vm.\sin(\omega.t) \\ eb &= Vm.\sin(\omega.t - 2\pi/3) \\ ec &= Vm.\sin(\omega.t + 2\pi/3) \end{aligned} \tag{28}$$

C. Simulation Parameters

All simulation parameters are grouped in the Table 3 below.

TABLE 3
SIMULATION PARAMETERS.

V_{ref} calculation	$V_{\text{m}} = 300.\sqrt{2}$ V
DC-bus voltage	E = 700 V
Sampling time	T_{S} = 0.4 ms
Switching frequency	Fc = 22.5 kHz
Transformer	Ration transformation = 1
Three-phase AC load	R = 72 Ω

D. Simulation results

The main result, concerning the advantage of the SVPWM application, is presented in the six curves of the three first figures (Fig.8, Fig.9, and Fig.10) showing respectively pulses (Sa_1, Sa_2), (Sb_1, Sb_2), (Sc_1, Sc_2). We can see clearly that switching are reduced to the 2 thirds of the pulse's period. Consequently, we wait to get less power switching losses. The two following curves (Fig. 11 and Fig. 12) present the advantage of multilevel inverters (with less harmonic contents injection) use. First, we can say that control strategy has operated at a satisfactory level. In fact, in the phase-to-fictive middle point voltage 'V_{ao}' and phase-to-neutral point voltage 'V_{an}', we see clearly the corresponding three-levels: (E/2→350 V, 0, -E/2→ -350 V) in the case of 'V_{ao}', (2.E/3→466,66 V, E/2→350 V, E/3→233.33 V) in the case of 'V_{an}'. Secondly, in Fig. 13 showing the harmonic spectrum of 'V_{an}', we measure a THD (given by (29)) of 19,44 % during the first 40 ms.

$$THD = \sqrt{\sum_{h=2}^{\infty} Van_h^2} \Big/ Van_1 \tag{29}$$

Where, h is the harmonic row.

Both Fig. 14 and Fig. 15 concern the supplied AC load (resistive load) represented by the voltage V_{load} and the current i_{load}.

Finally, we end with the curve displayed in Fig.16 mentioning the DC-bus voltages V_{c1}(t) and V_{c2}(t). The two signals oscillate around a fixed value 350 V corresponding to E/2, but with enough ripples necessitating restriction in future works.

V. Conclusion

In this paper, a theoretical study concerning the application of the SVPWM control strategy on the three-level voltage inverter was presented. This last aimed on the one hand to prove the effectiveness of the SVPWM in the contribution in the switching power losses reduction,

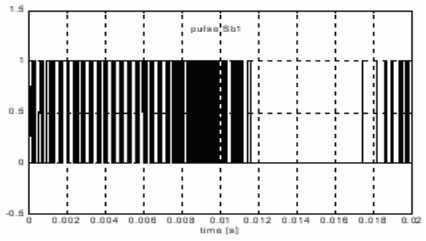


Fig. 8. Leg a upper's switches pulses Sa_1, Sa_2

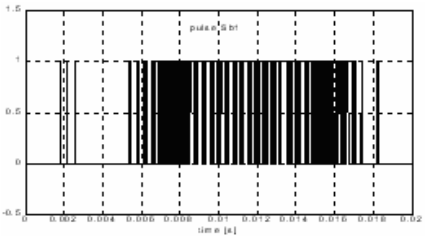


Fig. 9. Leg b upper's switches pulses Sb_1, Sb_2

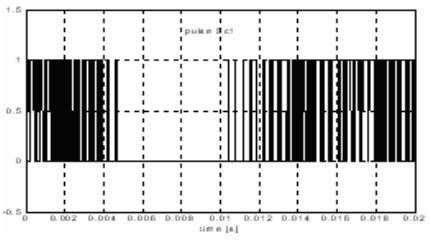


Fig.10. Leg c upper's switches pulses Sc_1, Sc_2

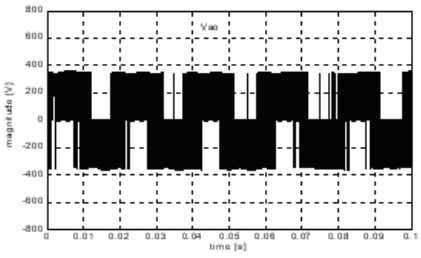


Fig. 11. Voltage *Vao.*

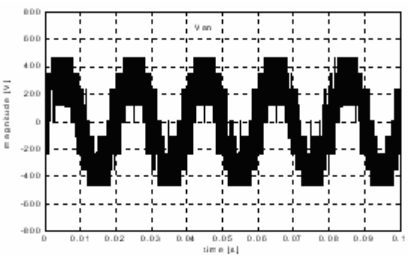


Fig. 12. Voltage *Van.*

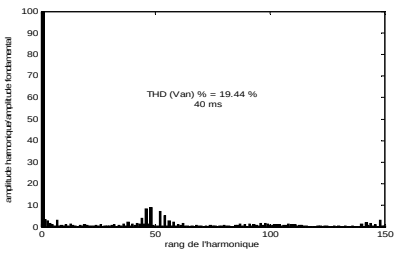


Fig. 13. *Van*. Harmonic's spectrum.

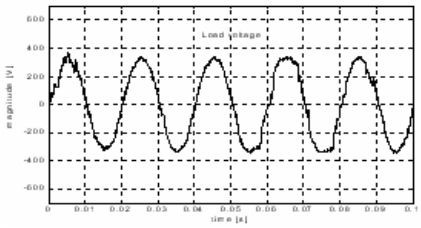


Fig. 14. Load voltage V_{load}

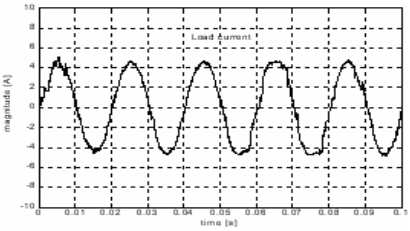


Fig. 15. Load current i_{load}

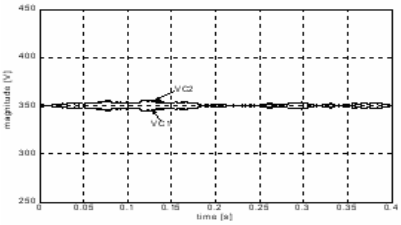


Fig. 16. DC-link voltages V_{C1}(t) and V_{C2}(t).

and to show the advantage of multilevel inverters that carry out voltages with less harmonic content's injection than the comparable two-level inverters on the other hand. The obtained simulation results were satisfactory. As prospects, future experimental works will validate the simulation results. Besides, we aim to include this study in a closed-loop system presented by a three-level active power filter.

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